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Low-Level RF Signal Processing Software

This note describes the software requirements for the low-level RF electronics which includes the Signal Processing Chassis and the Phase Detector Assembly. The Signal Processing Chassis contains the RF electronics to create an RF output with arbitrary phase modulation. The Phase Detector Assembly contains the RF electronics to precisely measure the amplitude and phase of eight RF input signals. Figure 1 depicts a simplified diagram of the low-level RF electronics, highlighting the interconnections.

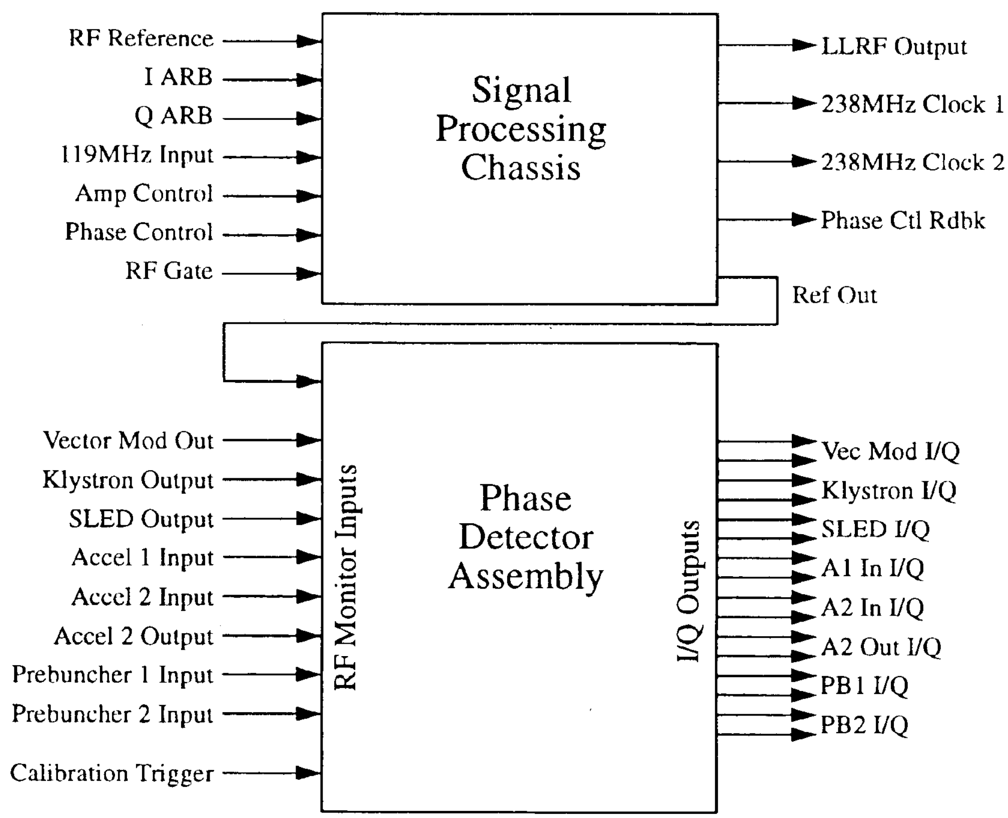

Figure 1. Diagram of low-level RF electronics

I/Q Monitoring - Phase Detector Assembly

There are eight I/Q demodulators within the Phase Detector Assembly. These I/Q demodulators are used to downconvert RF signals for precision amplitude and phase measurements. The RF signals being measured are delivered from various monitor points in the RF system: Vector Modulator Output, TWT Output, Klystron Output, Sled Output, Accelerator 1 Input, Accelerator 2 Input, and Accelerator 2 Output (Prebuncher 1 Input and Prebuncher 2 Input are also required for injector station). The eight pairs of downconverted I/Q signals from one Phase Detector Assembly are multiplexed into two digitizer channels. Each digitizer channel is multiplexed in a manner that allows simultaneous sampling of the I and Q signals from one demodulator. The software operations performed upon the I/Q data include data correction, data conversion, and data storage or display. Figure 2 shows the algorithm for this software operation.

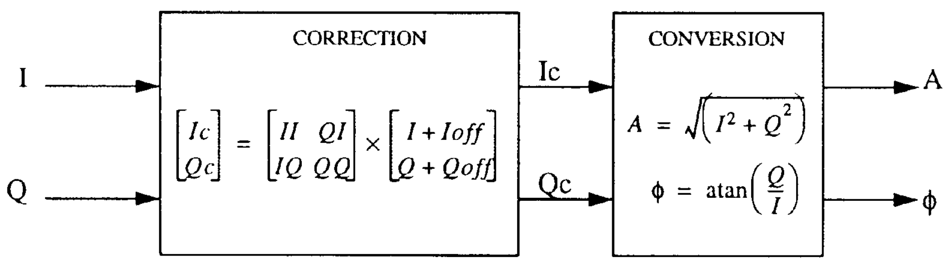

Figure 2. Software algorithm for I/Q demodulator

The data correction step consists of four multiply and two add operations. The six constants used in this correction (II, QI, IQ, QQ, Ioff, and Qoff) are determined by a calibration algorithm that is described later. The data conversion step performs the non-linear operations that convert I/Q to amplitude/phase. In addition, the data conversion step might include the scaling and other mathematical operations needed to convert the values to real engineering units. Note that the algorithm in figure 2 is performed upon each measured I and Q data sample, or approximately 1500 times (1.5 µs/1 ns) for each pair of captured I/Q waveforms. Because this may require an excessive amount of processor bandwidth, an alternative is proposed. The I and Q inputs from the digitizer consist of 8-bit data. If these two 8-bit I/Q values are used together as a 16-bit address for a look-up table, the entire algorithm can be accomplished in a single addressing operation. The generation of the look-up table would require some processor computation, but this is done infrequently as part of the calibration procedure. Because the amplitude and phase outputs require more precision that 8-bits, they should be stored as 16-bit values in the look-up table. The memory requirement for the look-up table is 128K 16-bit words per I/Q demodulator (or 1024K 16-bit words for 8 demodulators). In summary, the software sequence for each I/Q monitoring channel is:

(1) Capture the I and Q waveforms associated with an I/Q demodulator. This provides 1500 8-bit data values for the I waveform and 1500 8-bit data values for the Q waveform.

(2) Convert the 1500 I/Q data pairs to 1500 A/ϕ data pairs using the calibration look-up table.

(3) Store the A/ϕ data in memory or transmit via the network for remote archival or display.

Calibration of an I/Q demodulator results in the look-up table that allows on-line data correction. This look-up table requires 128K 16-bit words of memory per I/Q demodulator so that every possible combination of 8-bit I data and 8-bit Q data has a corresponding 16-bit amplitude and 16-bit phase associated with it. Within the hardware, the calibration trigger switches on an 11.414 GHz source that is coupled into the RF input of the I/Q demodulator. This calibration source is switched on between the regular RF pulses when normal RF signals are not present. The calibration signal is offset by 10 MHz from the RF center frequency, resulting in 10 MHz sinusoids on the output I and Q signals from the I/Q demodulator. The calibration signal is gated on for approximately 1 μs, or ten complete cycles of the 10 MHz sinusoids. There signals are captured by the VXI digitizer which is triggered synchronously with the calibration source. Figure 3 shows an example of the I and Q waveforms generated during calibration. With ideal I/Q demodulators, the sinusoids would be equal in amplitude, with zero DC offsets, and with exactly 90 degrees of phase between them. The non-ideal sinusoids captured during calibration are evaluated to characterize the inherent errors of the I/Q demodulator.

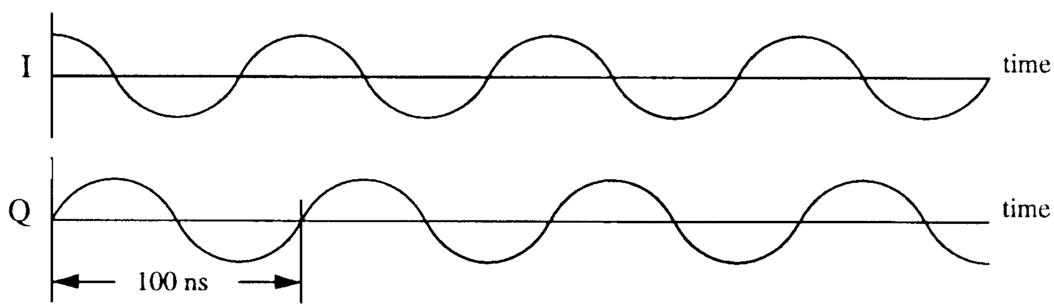

Figure 3. Sinusoidal I and Q outputs during calibration

If the I and Q sinusoidal frequency, w, is not known exactly, it can be determined in software by measuring the time interval between zero crossings to give the period of the sinusoids. For each sinusoid, a curve fitting algorithm should be used to fit the I and Q signals into the form:

$$I(t) = A_I \cos(wt) + B_I \sin(wt) + C_I$$

$$Q(t) = A_Q \cos(wt) + B_Q \sin(wt) + C_Q$$

Once the curve-fitting algorithm converges upon a result, the six identified parameters (A_I, B_I, C_I, A_Q, B_Q, C_Q) are used to calculate the six correction constants (II, QI, IQ, QQ Ioff, and Qoff) as follows:

$$R_I = \sqrt{A_I^2 + B_I^2} \qquad \phi_I = \operatorname{atan}\frac{-B_I}{A_I} \qquad R_Q = \sqrt{A_Q^2 + B_Q^2} \qquad \phi_Q = \operatorname{atan}\frac{-B_Q}{A_Q}$$

$$\Delta A = \frac{R_I}{R_Q} \qquad \Delta\phi = \phi_I - \phi_Q - 90°$$

$$II = \frac{\cos\frac{\Delta\phi}{2}}{\cos\Delta\phi\sqrt{\Delta A}} \qquad IQ = \frac{\sin\frac{\Delta\phi}{2}}{\cos\Delta\phi\sqrt{\Delta A}} \qquad QI = \frac{\sqrt{\Delta A}\sin\frac{\Delta\phi}{2}}{\cos\Delta\phi} \qquad QQ = \frac{\sqrt{\Delta A}\cos\frac{\Delta\phi}{2}}{\cos\Delta\phi}$$

$$Ioff = -C_I \qquad Qoff = -C_Q$$

These constants (II, QI, IQ, QQ, Ioff, and Qoff) are used to generate the look-up table using the algorithm represented in figure 2. The look-up table consists of amplitude and phase values that have been computed with this algorithm for every possible combination of I and Q data. The combined 8-bit I value and 8-bit Q value is used as the 16-bit address for the look-up table which contains the corrected 16-bit amplitude and 16-bit phase values.

The LLRF system is designed to insure that the correction constants remain stable and constant over the range of RF input signal levels. If the characteristics of the I/Q demodulators vary with RF signal level, a VXI microwave source can be used to generate calibration signals at various amplitudes, at which correction constants can be calculated. This allows the same type of calibration and correction with some additional complexity.

I/Q Modulator - Signal Processing Chassis

There is one I/Q modulator within the Signal Processing Chassis. This I/Q modulator is used to upconvert baseband I/Q signals into an appropriately phased RF signal to drive the TWT and subsequent klystron. Because the klystron is operated in saturation, the I/Q modulator is used as a fast phase shifter only, with its RF output kept at a constant power level. Because we can characterize the I/Q modulator very accurately for a single RF output level, a look-up table can be used to correct the inaccuracies in the I/Q modulator. In the laboratory, we can experimentally determine the list of I and Q values that create an RF signal with constant amplitude for all possible phase angles in 0.088 degree increments (360 degrees/2^{12}). This allows the I/Q modulator correction algorithm to be implemented in a 8K word look-up table that uses a 12-bit phase value as an address to define two 16-bit data values for I and Q. By simplifying the I/Q correction to a look-up table, the correction algorithm can be accomplished by a simple read operation in which any phase input provides corrected I and Q outputs. Ultimately, two Arbitrary Function Generators produce the I and Q waveforms required for pulse compression from a sequence of I data values and a sequence of Q data values. These I and Q data sequences each consist of approximately 357 (1.5 µs/4.2 ns) data values.

Real-time adjustments of the station phase must be provided to allow an operator to manually tune the station phase or to allow a feedback loop to automatically correct for phase drifts. In order to accomplish this, the station phase adjustment has been divided into two hardware devices: a fixed phase setpoint incorporated in the Arbitrary Function Generator waveforms and an analog phase shifter that allows +/- 30 degrees of phase adjustment to be performed in real-time. The fixed phase setpoint incorporated into the Arbitrary Function Generators is accomplished in software during initial turn-on and remains fixed thereafter. Real-time adjustments of +/- 30 degrees around the station phase setpoint are accomplished with an analog phase shifter that is driven by a Camac DAC module. This analog phase shifter allows an operator to adjust a knob and see phase changes occur in real-time or a feedback loop to compensate for phase drifts. By defining the pulse compression phase shift waveform as a sequence of 357 phase values allows the station phase setpoint to be added as a fixed value to each of the 357 phase data points. Consequently, a change in the station phase setpoint or a change in the pulse-compression phase waveform is accomplished through the following software steps:

(1) Add the station phase setpoint to the phase value for the 357 data points in the pulse compression waveform.

(2) Use the phase sum of (1) to address a look-up table containing the appropriate I and Q values for each of the 357 data points.

(3) Down-load the 357 I data values and 357 Q data values into the two Arbitrary Function Generators.

This sequence of operations is performed infrequently as part of the setup procedure to identify the station phase, or when a new phase compression waveform has been calculated.

Timing and Multiplexing

There is one Camac Simple Timing Buffer (STB) card per RF station that provides the NIM-level triggers that are used for synchronization. The timing signals required for one RF station are listed in table 1. Six of these timing signals are related to the low-level RF signal processing including the VXI Digitizer Trigger (PP), the VXI Digitizer Trigger (TRBR), the Calibration Trigger, the ARB Trigger, the LLRF Start Trigger, and the LLRF Stop Trigger. The VXI digitizer trigger (PP) starts the VXI digitizer data acquisition cycle for a pulse pattern associated with a special beam code activity. The VXI digitizer trigger (TRBR) starts the VXI digitizer data acquisition cycle at the normal machine repetition rate. The Calibration Pulse enables the on-line calibration of the I/Q demodulators by switching on a calibration source and by initiating a data acquisition cycle in the VXI digitizer to acquire the calibration waveforms. The three aforementioned triggers are all used to trigger the VXI digitizers under different operating conditions. Consequently, a multiplexer is used to switch between the three possible digitizer triggers for the different conditions: beam-code related data acquisition, normal machine data acquisition, and calibration data acquisition. A rising edge on the selected VXI digitizer trigger starts the data acquisition cycle for a duration defined by the digitizer software. The ARB Trigger initiates the

Arbitrary Function Generator waveform outputs that are used to create the correct phase modulation on the LLRF. A rising edge on the ARB Trigger starts the waveform generation cycle for a duration defined by the ARB software. The LLRF Start Trigger and LLRF Stop Trigger are used by the RF Trigger Chassis to create the RF Gate pulse. This RF Gate is used by the RF Signal Processing Chassis to pulse-modulate the LLRF output.

There are two analog multiplexers within the VXIbus chassis to support the eight I/Q demodulators in the Phase Detector Assembly. In addition to multiplexing the three triggers for the digitizer, these VXI modules are used to multiplex the eight pairs of I and Q waveforms into two digitizer channels. In order to accurately measure phase over wide bandwidths, the propagation times for the I and Q channels should be closely matched. Phase measurements with signal bandwidths around 100MHz require that the propagation delays be matched to a fraction of 1 ns. One nanosecond difference in the propagation delays will cause 36 degrees of phase error in the 100 MHz signal components. Consequently, a calibration algorithm may be necessary to offset any differences in propagation delays.

#	TRIGGER FUNCTION	DESTINATION	COMMENT
0	Reserved for PAU	Reserved (Unused)	
1	VXI Digitizer (PP)	VXI Digitizer #1 VXI Digitizer #2	Repeated on beam code pulse pattern
2	VXI Digitizer (TRBR)	VXI Digitizer #1 VXI Digitizer #2	Repeated at normal machine rep rate
3	Calibration Trigger	Signal Processing Chassis VXI Digitizer #1 VXI Digitizer #2	Enable calibration source for demodulators
4	ARB Trigger	ARB #1 ARB #2	Initiates ARB waveform outputs
5	GPIB Oscilloscope	RF Station Oscilloscope	Repeated at ~ 30 Hz
6	Command Charge	RF Trigger Chassis	5ms prior to RF pulse
7	Modulator Trigger	RF Trigger Chassis	Fires Thyratron
8	TWT Trigger	RF Trigger Chassis	Starts TWT Gate
9	LLRF Start Trigger	RF Trigger Chassis	Starts LLRF output
10	LLRF Stop Trigger	RF Trigger Chassis	Stops LLRF output
11	Peak & Hold Trigger	RF Trigger Chassis	Resets Peak & Hold
12	GADC Enable	RF Trigger Chassis	Enables GADCs
13	GADC Ch. 0-2	Camac GADC Ch. 0 Camac GADC Ch. 1 Camac GADC Ch. 2	Triggers Ch. 0-2
14	GADC Ch. 3-5	Camac GADC Ch. 3 Camac GADC Ch. 4 Camac GADC Ch. 5	Triggers Ch. 3-5
15	REUS	Reserved	360 Hz trigger

Table 1: STB timing signals for one RF station