Copyright 1999 Society of Photo-Optical Instrumentation Engineers

This paper was published in the 1999 SPIE Conference Proceedings and is made available as an electronic reprint with permission of SPIE. Single print or electronic copies for personal use only are allowed. Systematic or multiple reproduction, or distribution to multiple locations through an electronic listserver or other electronic means, or duplication of any material in this paper for a fee or for commercial purposes is prohibited. By choosing to view or print this document, you agree to all the provisions of the copyright law protecting it.

Design of a Test System to Characterize Very High-Frequency Ultrasound Transducer Arrays

 R.L. Tutwiler, Applied Research Laboratory, The Pennsylvania State University S Madhavan, K.V. Mahajan, University Department of Electrical Engineering, The Pennsylvania State University Department of Electrical Engineering P.O. Box 30 State College, PA. 16804

ABSTRACT

A flexible test system is described that has the capability to characterize very high frequency ultrasound transducer arrays up to 128 elements. The system has the capability of testing single element transducers as well as groups of array elements. The R.F. front end electronics consists of pulser circuit, preamp and time gain compensation circuit. The pulser circuit is a high voltage, high speed, switching circuit designed for -60 V pulse amplitude and pulse width as low as 10 ns. The preamp is a low noise, wide bandwidth amplifier and the time gain compensation circuit has a low noise figure and a bandwidth of 75 MHz. Custom, miniaturized PCB's have been fabricated and tested for the R.F. electronics. The data acquisition system has the capability to synchronously sample 8 channels at 250 MHz, or 16 channels at 125 MHz with 8 bit resolution. Multiplexing and demultiplexing units have been designed and tested for all the 128 channels. The demultiplexers are suitable for frequencies up to more than 100MHz, and the multiplexers have a bandwidth of 700MHz with good off isolation and cross talk. The multiplex/demultiplex architecture gives the test system the capability to perform synthetic aperture processing as well as dynamic apodization. An adapter board interfaces the external components to the PC (digital I/O card). A software control structure for control and synchronization of the system components for 128 elements has been designed and developed. Results are shown for the characterization of individual 50 MHz transducers as well as element responses for a 30 MHz array.

KEYWORDS

Medical Ultrasound, transducer, linear array, pulser, receiver, TGC, time-gain compensation, multiplexer, de-multiplexer, synthetic aperture, dynamic apodization

1. INTRODUCTION

This paper discusses the design and development of a single channel transceiver for broad bandwidth ultrasound imaging equipment for medical applications. Its design is being used in the development of a 128-channel ultrasound imaging equipment. The transceiver has the pulser as transmitter and a broad bandwidth receiver. A high frequency ultrasound transducer is used both for the transmission of ultrasound pulse and for receiving the ultrasound echoes. The performance characteristics of both 50 and 30 MHz transducers developed at the NIH Transducer Center at the Pennsylvania State University are tested and calibrated. A single channel system is illustrated in figure 1. The diode expander, a MATEC DEX-3, prevents noise from the pulser electronics to reach the receiver. The diode limiter DL-1, MATEC, protects the receiver circuitry. A generalized structure of the 128 channel system that is composed of the individual components is shown in figure 2. The arbitrary waveform generators are used for transmit/Receive systems are computer controlled via a digital I/O card.



Figure 1. Single Channel Test System Block Diagram

All systems and circuits prior to design are simulated in PSPICE. Figure 3 depicts a single channel Transceiver where the system transducer is analyzed using a Redwood model [1]-[3].



Figure 2. 128 channel system block diagram



Figure 3. Spice Schematic for A Single Channel Transceiver

2. PULSER CIRCUITRY

The pulser design specifications are as follows:

Pulse amplitude: -60 V

Pulse width: 20 ns

An extensive literature search was done on existing methods of pulser design. An application note published by Supertex Inc was used as a reference [4]. The design was first implemented in SPICE and found to meet specifications. The circuit is as shown below in figure 4.



Figure 4. Pulser Circuit

The circuit was assembled on a copper clad board. The input Vin to the circuit is a 2.5 V amplitude TTL square wave, 20 ns pulse width with a variable pulse repetition frequency (PRF). The output was observed on an oscilloscope and matched the expected results from simulations. Almost all the devices used in the copper clad assembly were obtained in surface mount packages and a miniature version of the circuit was made. This circuit board is shown in figure 5.



Figure 5. Pulser PCB Layout

3. RECEIVER CIRCUITRY

The receiver circuit interfaces to the transducer through the limiter. The output of the limiter is fed to a preamplifier. A non-inverting configuration of an operational amplifier is used as the preamplifier. The part chosen for the preamplifier is a MAX4106 operational amplifier made by Maxim Integrated Products. The MAX4106 operational amplifiers combine high-speed performance with ultra-low-noise performance $0.75 \text{nV}/\sqrt{\text{Hz}}$. The preamplifier is set for a gain of 14dB. The output of preamplifier is fed to a variable gain amplifier (VGA). The AD603 made by Analog Devices is the variable gain amplifier used. Its gain is set by a dc voltage (-500 mV <= VC <= 500 mV) applied to the control port. The total gain range is from – 11dB to 31 dB. The output of the variable gain amplifier is a ramp (-500 mV <= VC <= 500 mV). The ramp repetition frequency for VGA control is a function of the pulser pulse repetition frequency. The ramp slope is a function of medium attenuation of the ultrasound, intensity variation in the ultrasound beam with distance and total round trip distance traveled by the ultrasound pulse. The function of this VGA is to do time gain compensation (TGC).

The receiver circuit was initially tested in SPICE. The circuit schematic used for testing is shown in figure 6.



Figure 6. Receiver Circuit

The receiver circuit was initially made using evaluation board kits supplied by the IC manufacturers. A miniature version of the receiver using only surface mount components was also made and tested. Figure 7a is the preamp board and figure 7b is the TGC layout.





Figure 7. a. Preamplifier PCB Layout

b. Time Gain Compensation (TGC) PCB Layout

The data acquisition system is depicted in figure 8. 250 MHz sampling frequency A/D cards made by Gage Applied Sciences are used for digitization of the raw RF data.



Figure 8. Gage Data Acquisition System Open Showing Compugen 1100 IBM PC Based High Speed Digital To Analog Converter Card

Sampled blocks of raw RF data for each channel are buffered and input to the MATLAB postprocessing routines. MATLAB was used to implement the functions of a band pass filter, full wave rectifier and a low pass filter on the raw RF data, for doing envelope detection. This processed data was further used again in MATLAB to generate an image of the phantom load. The final objective is to replicate the successfully tested single channel transceiver to be used for the implementation of a 128-channel system.

4. CONTROL STRUCTURE

The system comprises of both the software and hardware. The control structure is implemented in software as C/C++ program. In accordance with the name, it performs the function of control and synchronization of all the internal and external components of the system. The AWG board, A/D array and the digital I/O board are interfaced with the control unit by ISA bus where the rest of the components are connected through these boards. It exploits the capability of the multiplexing and demultiplexing units to provide flexibility to the system i.e. the control signals are generated based on the selected test scheme. The control structure provides the flexibility to test system to perform synthetic aperture processing by selecting the individual elements from left to right or vise a versa in groups of eight or 16 elements, as well as from

the central group to the end of the array. Dynamic apodization processing is performed by selection of elements from the center element through outward elements in both directions, in a continuous fashion.

The test schemes include transmit on \mathbf{n} and receive on \mathbf{n} configuration, and transmit on **one** and receive on \mathbf{n} configuration for synthetic aperture processing. In the case of dynamic apodization processing, the focal distance is changing over time till all the elements in the array are covered.

In transmit on **one** and receive on **n** configuration, only one of the demultiplexers is in an enable state while all the others are in a disable state. In order to have equal distribution of the transmitted energy on the array elements from the selected group, the central element of that group is selected as the element to be transmitted on and the corresponding demultiplexer is enabled. At the same time, it is possible to select all the elements of the group, with transmit on one element at a time. But this results in an extremely slow operation as the complete process is performed recursively and hence more time is required to complete the scan.

Under transmit on \mathbf{n} and receive on \mathbf{n} configuration, the transducer array elements selected for transmit are also selected for receive. The control signals to both, the multiplexing and the demultiplexing units are identical.

5. MULTIPLEXING AND DEMULTIPLEXING

In order to test transducer arrays up to 128 elements with the available number of channels (8 in single channel mode and 16 in dual channel mode of A/D cards), it is necessary to provide the hardware to allow the spanning of all the elements. This is provided with the demultiplexer unit in the transmit chain and the multiplexer unit in the receive chain. Since up to 128 elements need to be spanned with 16 channels, the demultiplexers and multiplexers are in 1:8 (1 input to 8 outputs) and 8:1 (8 inputs and 1 output) configurations respectively. The design of this unit involved several considerations.

The multiplexing and demultiplexing units are designed to operate at higher frequencies (in the order of 50 MHz and more) and offer higher noise immunity because of the signal voltage levels involved. The important factors that are considered in the design are:

- 1. R_{ON}: The "on" channel resistance
- 2. Leakage currents
- 3. Charge Injection
- 4. Cross talk and OFF Isolation
- 5. Wide band operation range
- 6. Response time and propagation delay

 R_{ON} value plays an important role in high frequency systems as the system needs to be impedance matched to maintain the signal integrity. In addition to this, the "on" channel resistance along with switch capacitance affects the multiplexer/demultiplexer response and hence affects the input signal. Thus capacitance consideration is also important along with channel resistance. To reduce the capacitive loading of the signal, a suitable multiplexer/demultiplexer configuration that reduces the number of channels in parallel, is required.

Leakage currents exists both when the multiplexer/demultiplexer is ON and OFF and are categorized as I_S (OFF), I_D (OFF), and total current I(ON). I(ON) is sum of both drain and source currents. They are at maximum when the input signal approaches the supply rails (as in case of demultiplexer). These currents with finite R_{ON} results in a voltage drop across the channel and thus causes the signal attenuation.

Charge injection is a phenomenon that results in spikes during switching. Since the switches operate at very high frequencies and the voltage levels are very low (especially in case of multiplexer), switching spikes result that are highly undesired. Thus, the charge injection, which is result of charge transfer when switching between ON and OFF states should be as minimum as possible.

Wide band operation requirement coincides with the need for a constant "on" channel resistance (R_{ON}). As already mentioned, since the received response from the transducer elements is wide band, it is critical for the multiplexer to possess a wide band operating range.

Similar to the above factors, the OFF isolation and crosstalk are important considerations as they affect the signal integrity. Their significance is even more pronounced at high frequencies, as with the increase in frequency, these factors degrade drastically and hence provide very poor signal integrity.



Figure 9. Synthetic Aperture Processing Implementation (Group 16 (SAP_16_L_R))

In figure 9 a 16-element array is considered instead of 128-element array as in actual case. The demultiplexers and the multiplexers are 1-to-4 and 4-to-1 respectively each in four numbers (in actual implementation there are 16, 1-to-8 demultiplexers and 8-to-1 multiplexers). The selection is in groups of 4 at a time (in the real system it is 16 at a time).

Initially, the address of all the demultiplexers as well as the multiplexers are made zero. This results in selection of the first four pulsers. In the second iteration, only the address of first demultiplexer (dmux#0) is incremented by one and for others it is unchanged. This causes the dmux#0 to select pulser#5 and not pulser#1. Thus pulsers 2 through 5 get selected. In the third iteration, only the address of dmux#1 is incremented and the pulsers, 3, 4, 5 and 6 get selected. Thus repetition of the same procedure (i.e. incrementing the address of one of the demultiplexers in sequence and keeping the address of the others unchanged), allows spanning over all the 16 elements in the desired manner. Therefore, when the address of all the demultiplexers is "11" in binary, the final four pulsers (and thus the elements) are selected.

The same mechanism is expanded to the actual implementation for the 128-element transducer array. In the case of multiplexers, instead of the pulser selection, corresponding pre-amplifiers are selected.

Figure 10 illustrates a group of 8 sub-configurations, in addition to changing the address of the multiplexers and the demultiplexers, the enable inputs to them also need to be changed in sequence. This introduces more complexity to the element selection mechanism and slows down the operation compared to the group of 16 operation. In the group of 16 sub-configurations, in transmit on \mathbf{n} and receive on \mathbf{n} mode,

the enable signals are not changed till the sequence is completed as both demultiplexers and multiplexers need to be enabled at the beginning of the sequence and disabled at the completion of the sequence.



Figure 10. Synthetic Aperture Processing Implementation (Group 8 (SAP_16_L_R))

A similar approach is used to explain the operation mechanism of SAP_16_L_R. The system consists of a demultiplexing scheme with four 1-to-4 demultiplexers and a 16-element transducer array. To resemble the selection of a group of eight elements at a time in this mode, the selection of a group of two elements (out of 4) at a time is done. To explain SAP_16_L_R mode, groups of 4 elements were considered to correspond to the groups of 16 elements for 128-element array. Thus in this case (SAP_8_L_R) to explain the groups of 8 mode, groups of two elements are considered.

As in the case of SAP_16_L_R mode, this case also implies that all the addresses are initialized to "00" but only the first two demultiplexers viz. dmux#0 and dmux#1 are enabled. This corresponds to selection of the first two elements. In the second iteration, dmux#0 is disabled and dmux#2 is enabled which selects the second and third elements and then dmux#3 is enabled and dmux#1 is disabled in the next iteration to select elements three and four. When all of the demultiplexers have the same address (which is only in the beginning), the enabling and disabling of the demultiplexers is performed in the sequence mentioned above. After this sequence is completed, only the address of the first demultiplexer is incremented and at the same time the same demultiplexer is enabled. While performing this operation, the demultiplexer that

was connected to the first element of the already selected group (which is dmux#2 in this case) is disabled. This procedure allows the progression of the sequence towards the right end of the transducer array.

7. EXPERIMENTS

To verify and test the design concept of the system for up to 128-element array, experiments were performed with two individual transducer elements in two different test configurations viz. with the multiplexing/demultiplexing of the channels, and without multiplexing/demultiplexing. For both the modes of testing, a flat reflector was used as the reflecting surface. Also the distance of the transducers from the reflectors was adjusted so that the returned echoes from these transducers are aligned in time.

7a. CHANNEL MULTIPLEXING/DEMULTIPLEXING SCHEME

This section describes the testing methodology and results for two-channel system with channel multiplexing/demultiplexing. Due to multiplexing of the channels, only one A/D board of the A/D array was utilized. It was configured to operate in single channel mode (i.e. sampling rate of 250 MS/s).

The test setup for this scheme is shown in figure 11.a. In this scheme, both the transducer elements are not exited at the same time, rather they are excited in sequence (i.e. they are multiplexed in time). In order to coincide with the synthetic aperture processing logic, the transducer selection was performed in both the directions. In one experiment transducer#1 was excited first and then the transducer#2 by sequencing the switching in that order. The other experiment performed switching in opposite direction. This corresponds to the selection of array elements from left-to-right and then right-to-left.

Other than the number of channels and elements, the functioning of rest of the system is the same as it would be for actual transducer arrays. In this setup too, the transmit signal from the AWG board is fed to the power amplifier (part of pulser) to obtain a 20ns negative going excitation pulse. The SYNC OUT of the AWG is delayed by using the delay generator. It is then provided as a trigger input to both, the AWG module and the A/D board for synchronization. The delay is adjusted first by providing a train of pulses to the pulser from the AWG card in the PC with very low pulse repetition frequency (PRF) (i.e. about 2 KHz,and then overlapping the output of the AWG module with the response from the transducers, on the oscilloscope.

Before this, the correct gain function for the TGC is determined by obtaining the control voltage values at points corresponding to the echoes. This gain function is then loaded into the nonvolatile memory of the AWG module using the software for loading the waveform. The duration and the amplitude of the control signal are entered from the front of the AWG module to generate the desired signal. In this experiment the duration was set to correspond to that for the first four received echoes.

7a.2. Two Independent Channel Scheme

In this scheme, two transducers were treated as two independent channels and hence no channel multiplexing/demultiplexing was required. The outputs of the two transducers were connected to two different A/D boards each configured to operate in single channel mode.

Since both the transducers were treated as individual channels, their excitation was carried out simultaneously. The test setup is shown in figure 11.b. As responses from both the elements are available at the same time, only a single iteration is necessary to perform as compared to four iterations in the previous scheme. The response from transducer-1 is fed to channel-1 and the second transducer was connected to



Figure 11. a. 2 Channel MUX/DEMUX b. 2 Channel Simultaneous sampling

channel-2 through the receive circuitry. The rest of the procedure and setting are the same including the duration of TGC amplifier gain control signal and the number of echoes. Instead of acquiring the echoes only once (i.e. performing single iteration), the response was acquired twice without any special purpose.

8. RESULTS

8a. CHANNEL MULTIPLEXING/DEMULTIPLEXING SCHEME

In order to test the switching mechanism along with the TGC action, the returned echoes were acquired by passing them through the pre-amplifier and TGC stages. The acquired responses shown in figure 12.a and figure 12.b. These figures demonstrate the switching between the elements in left-to-right (transducer-1 and transducer-2) and right-to-left (transducer-2 and transducer-1) direction respectively. The time gain compensation of the returned echoes is also evident from figures as the amplitude of the returned echoes remains almost the same at all the times.

The gain function corresponding to transducer-2 was provided to both the TGC amplifiers. The plot in the figures also shows the difference in the sensitivities of the transducers. Thus it can be concluded that the transducer-1 has very low sensitivity.

8a.2. Two Independent Channel Scheme

Implementation of this scheme allowed testing of the system in multi-channel mode and also ensured that the data can be acquired simultaneously in multiple channels in a desired manner. The system synchronization and operation is observable through the figures 12.c and 12.d for transducers 1 and 2 respectively.



Figure 12. 50 MHz Transducer System Response Curves

The following two figures illustrate the expanded version of the above figures for an experimental 50 MHz transducer that was designed at the NIH center. The utility of the test systems allows complete characterization of the impulse response as shown in figure 13. The top part of figure 13 is a multiplexed pulse of the two channel test system that was multiplexed from Left to Right. The bottom part of the figure is a multiplexed pulse that was multiplexed from Right to Left. Figure 14 shows two elements from an experimental 4channel 30 MHz array [5] and their respective impulse responses.



Figure 13. Impulse response of 50 MHz Transducer elements



Figure 14. Impulse response of 50 MHz Transducer elements

CONCLUSIONS

A flexible test system is described that has the capability to characterize very high frequency ultrasound transducer arrays up to 128 elements. The system has the capability of testing single element transducers as well as groups of array elements. It has the capability to perform synthetic aperture processing as well as dynamic apodization. The system will be used to characterize system performance, sensitiviy, and imaging capabilities.

REFERENCES

[1] Morris SA, Hutchens CG, "Implementation of Mason's Model on Circuit Analysis

Programs," IEEE Trans. Ultrasonics, Ferroelectrics, and Frequency Control,

Vol. UFFC-33, No. 3, 295-298 (May 1986).

[2] Ritter TA, Private Communication on SPICE Implementation of Redwood Model (1997)

[3] Van Tol DJ, Private Communication on Transducer Modeling (1997).

[4] Supertex Inc VN/VP13 Series Application Note AN-D8 1996]

[5] 30 MHz Medical Imaging Arrays Incorporating 2-2 Composites, T. Ritter, K.K. Shung, X. Geng, H.

Wang, and T.R. Shrout, 1998 Ultrasonics Symposium, Japan

[6] S. Moore, "Designing with Analog Switches", Marcel Dekker, Inc., 1991.

[7] "CompuGen 1100 Hardware Manual and Installation Guide", Gage Applied Sciences Inc.

[8] "PCI-20378W-1 Buffered 240-Channel Digital Input/Output Board and PCI-20369S Mater Link Software Libraries Manual", Intelligent Instrumentation.

[9] "CompuScope 2125 Hardware Manual and Installation Guide", Gage Applied Sciences Inc.

[10] "DG535 Digital Delay/Pulse Generator Operating Manual and Programming Reference", Stanford Research Systems, Inc.