3D Detector/Electronics Integration Technologies - Applications to LC, SLHC and Photon Sources

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Contents:

- The next generation of facilities ILC, CLIC, μCOLL and LHC
- Physics Environment
- Detector Constraints
  - Power and noise
  - Radiation resistance
  - Mass
- Introduction to 3D IC Technologies
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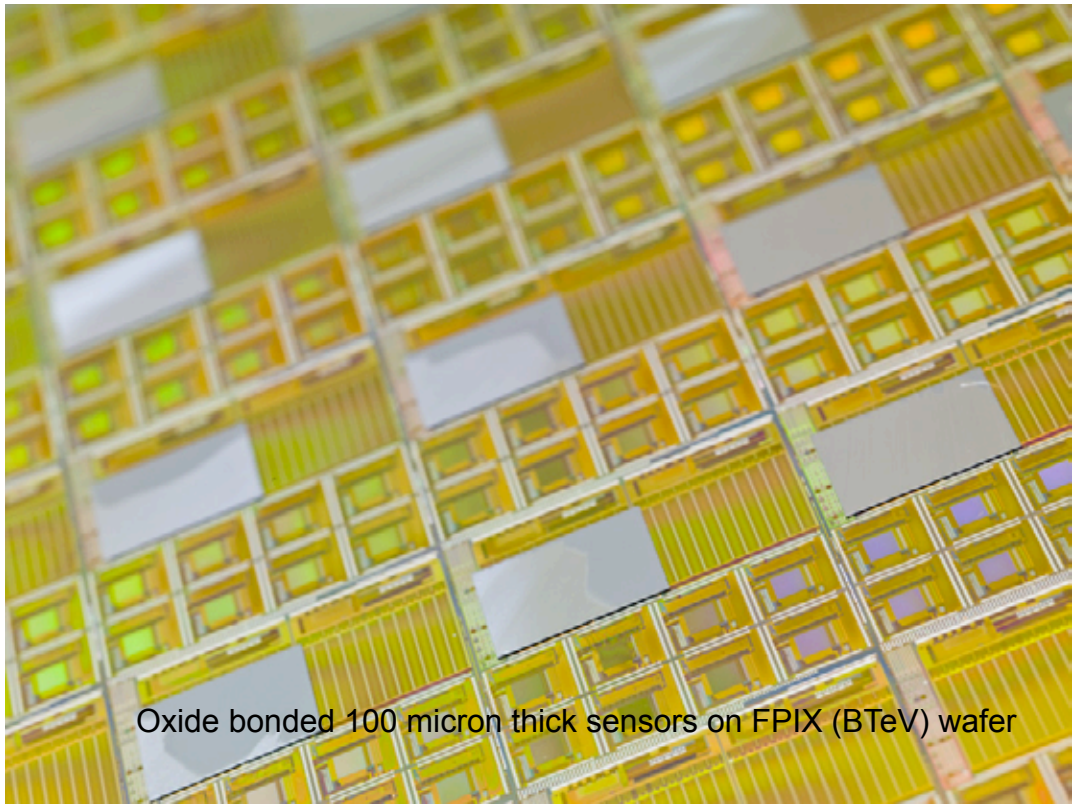
- 3D Development
  - Oxide bonding
  - VIP Chip for ILC
  - Tezzaron 3D IC
- Application to X-ray Correlation spectroscopy
- Application to sLHC Track Trigger
- Conclusions



Oxide bonded 100 micron thick sensors on FPIX (BTeV) wafer

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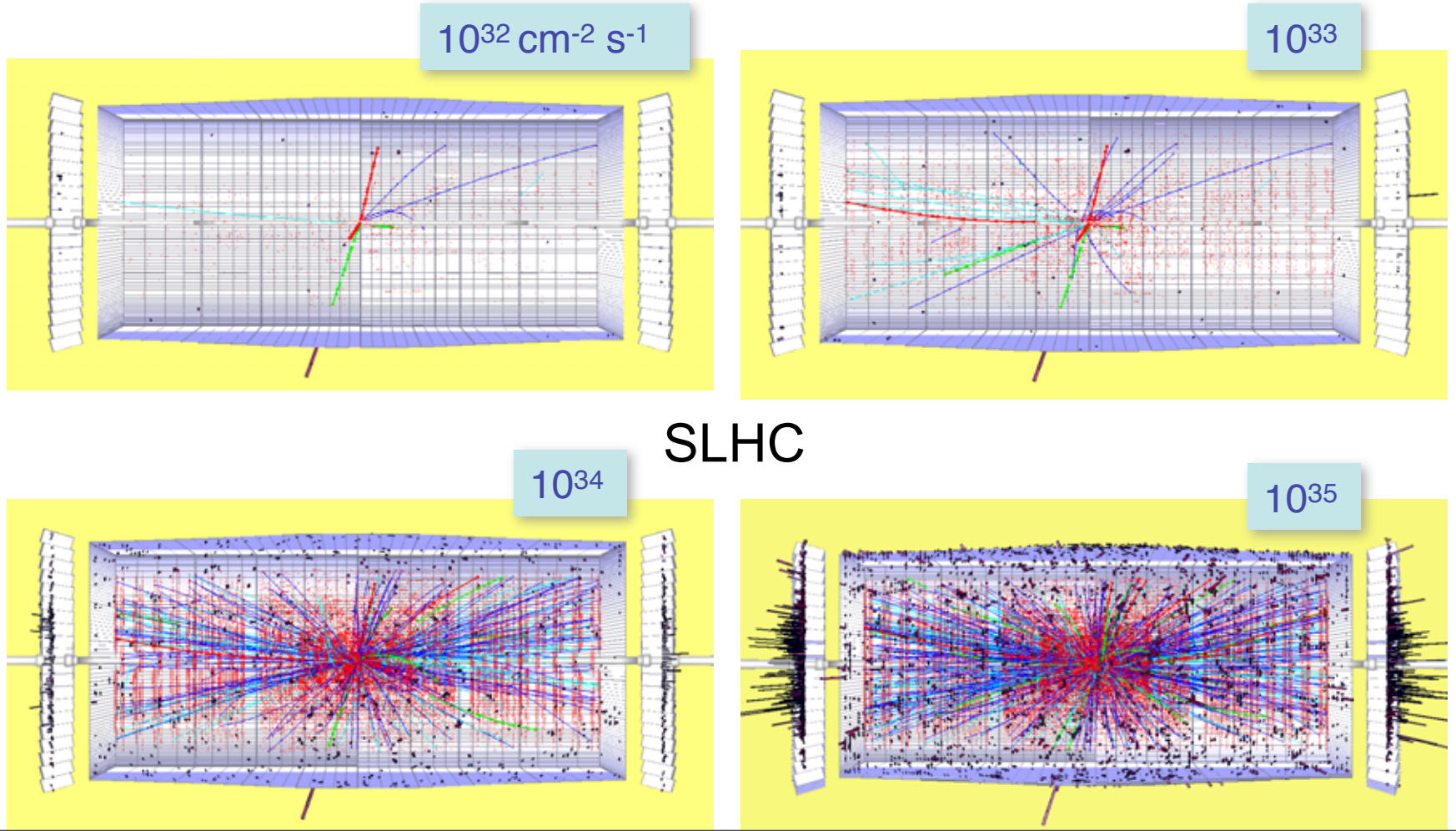
The Vertex Detector Commandments

1. Thou shalt minimize mass
- Thou shalt have high bandwidth
- Thou shalt be radiation hard
- Thou shalt not dissipate power
- Thou shalt have complex functionality
- Thou shalt maximize resolution
- Thou shalt minimize dead regions
- Thou not covet thy neighbors signals

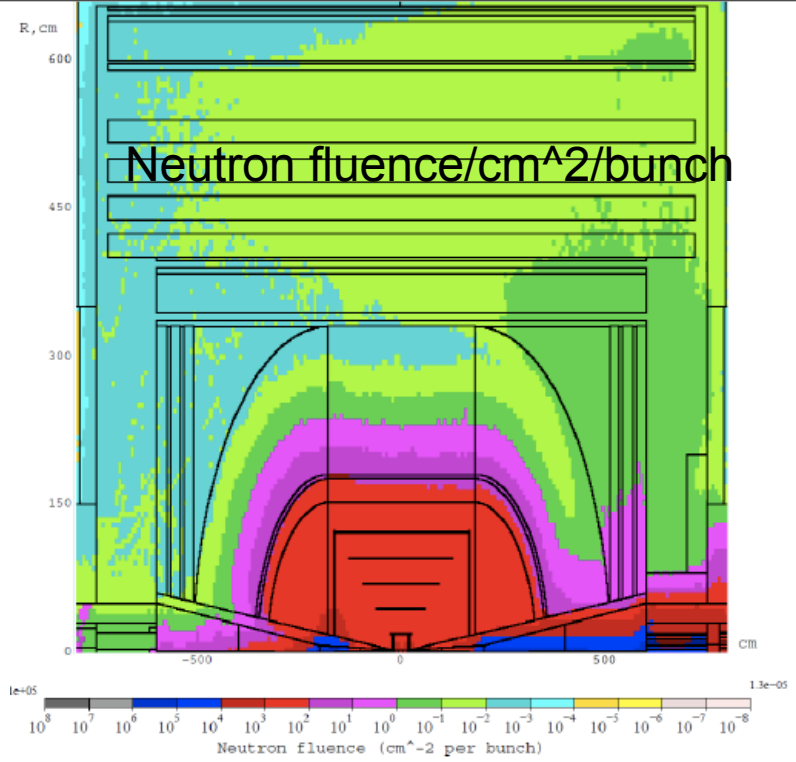
That's all I came up with, you are free to add 9 and 10 at the end of the talk

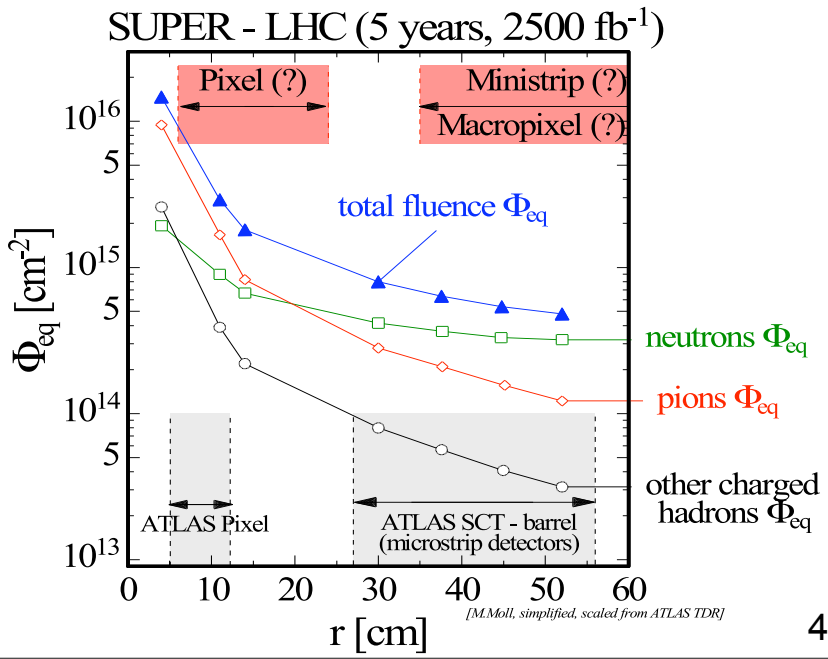
- The next generation of experiments will face unprecedented challenges
  - At the sLHC, with luminosities of 10^{35} with ~400 interactions/25 ns crossing
  - At the ILC or CLIC or muon collider where there will be a premium on precision measurements in difficult environments
  - Fast, time stamping detectors for x-ray focal planes



Palette of Future Detectors

- ILC Vertex Detector
  - Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
  - Transparency ($\sim 0.1\%$ X_0 per layer)
- Muon Collider
  - 1-3 TeV muon collider on FNAL site
  - Many accelerator issues
  - Substantial detector and radiation backgrouns
- CLIC
  - Challenging time resolution
- SLHC
  - 200-400 int/25 ns crossing
- X-Ray Imaging
  - Variety of challenges - timing

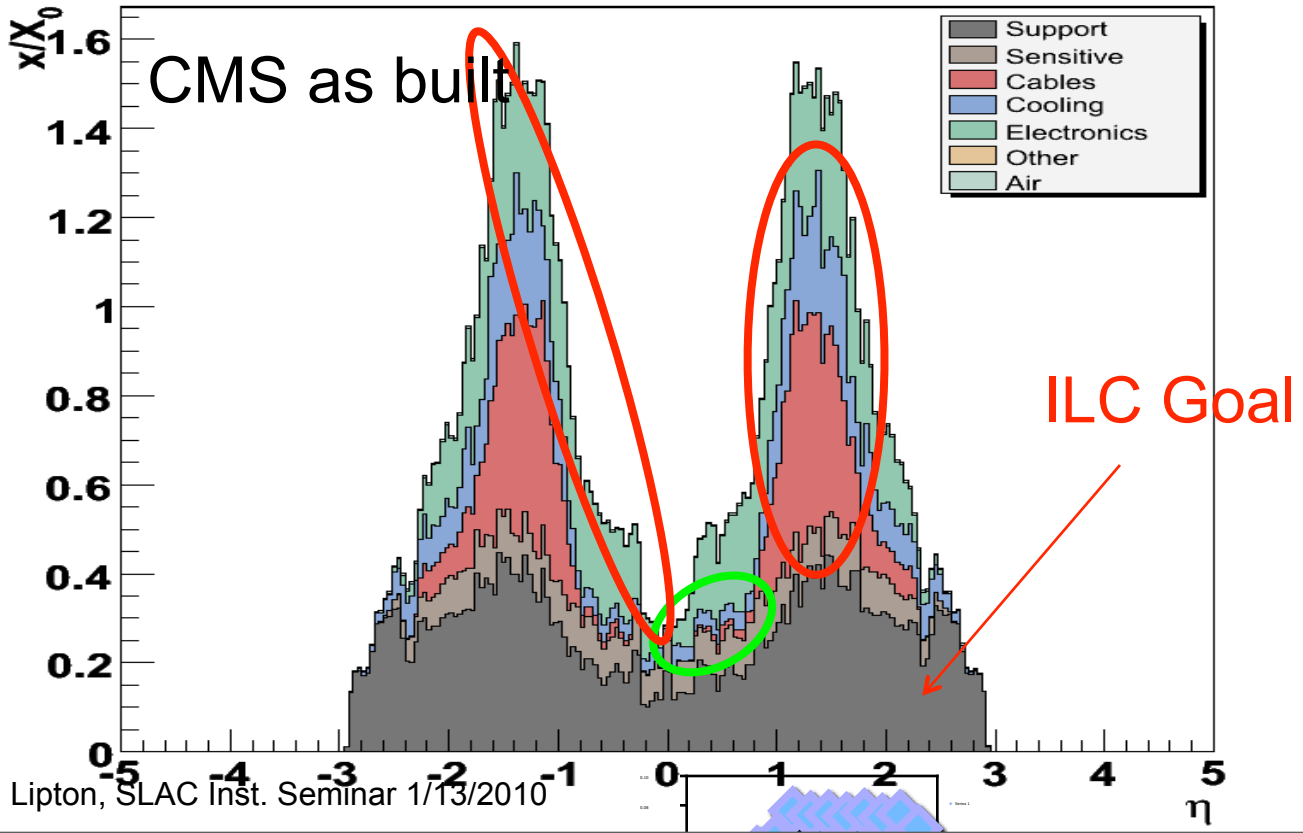




Detector Mass

Mass Drivers:

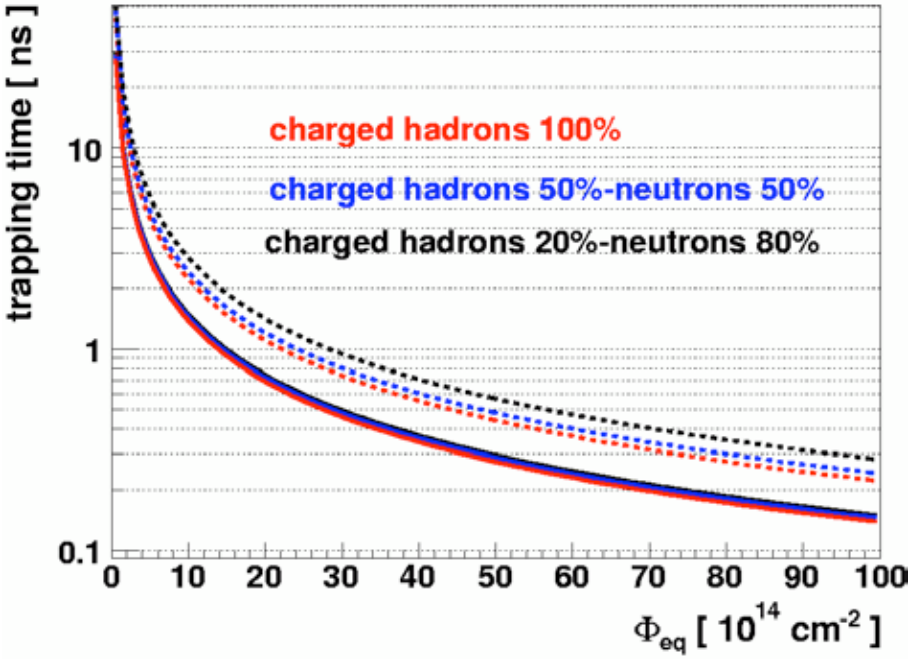
- Cooling and associated infrastructure – directly related to power dissipation and radiation damage which forces low temperature operation
- Supports
- Cables, interconnects and electronics

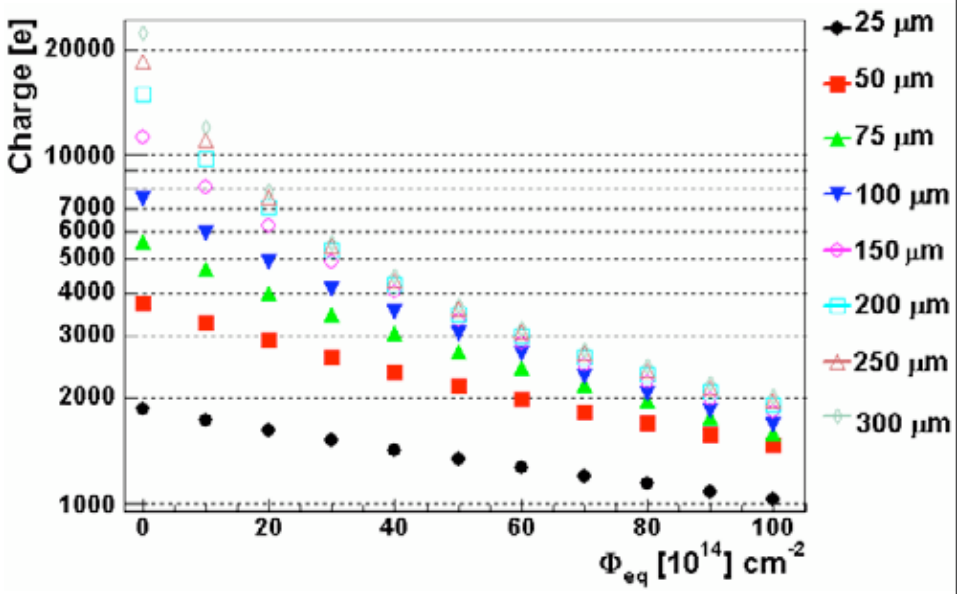


Thinned Detectors and Radiation Tolerance

- Radiation reduces the mean free path of charge carriers in silicon
  - Thinned detectors collect almost as much charge as thicker detectors after irradiation
  - Depletion voltage is much lower (V_d~thickness^2)
  - Leakage current is lower ~ t
- Of course the initial signal is 3-6 times lower …
- For ILC mass of detector itself (50 vs 300 μm) is important

3D detectors (Parker, Kenny) address this problem using deep etching 3D technology





(G. Kramberger)

Noise and Power

	# Pixels / chip	Pixel area [mμ²]	Idig [mA]	Iana [mA]	Power/ chip [mW]	Power/ pixel [μW]	Power density [mW/cm²]
ALICE	8192	21'250	150	300	810	99	466
ATLAS	2880	20'000	35	75	190	67	335
CMS	4160	15'000	32	24	121	29	194
CMS no on-chip regulators					87	21	142

(R. Horisberger)

- Noise scales as C and $1/\mathrm{sqrt}[g_m\tau]$, $g_m \sim (I_d/nV_T)$.
- For a strip or pixel detector for a given noise
  - $I \sim C^2$, $P \sim C^2$
  - C ~ (width/pitch) x length (modulo edge effects)
- If divided into n pixels/strip of spacing p x p (ignoring perimeter effects)

$$C_{strip} \cong k\frac{w}{p}l, \quad P_{strip} \propto \left(k\frac{w}{p}l\right)^2$$

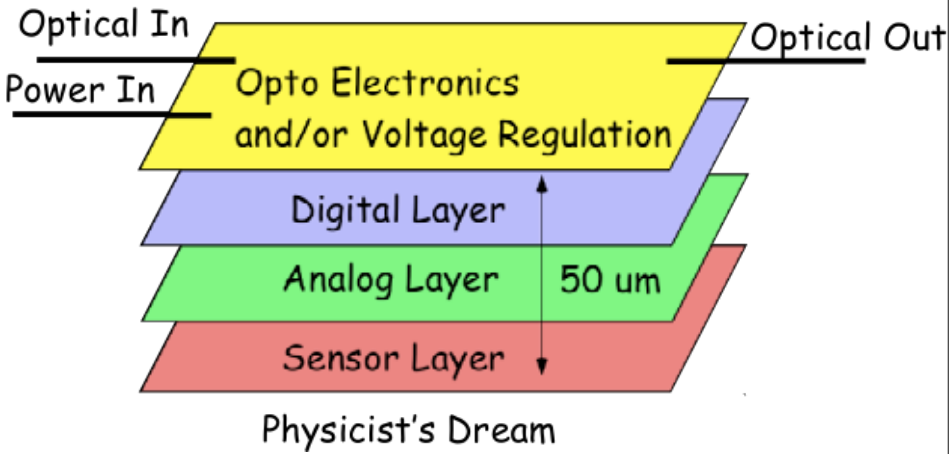
$$C_{pixel} \cong k\frac{w}{p}p, \quad P_{n\,pixels} \propto \left(k\frac{w}{p}l\right)^2\frac{p}{l}, \quad P_{n\,pixels} \cong P_{strip}/n$$

where factor depends on edge effects, overhead, and non front-end power. (Spieler estimates f to be about 4 for front ends.)

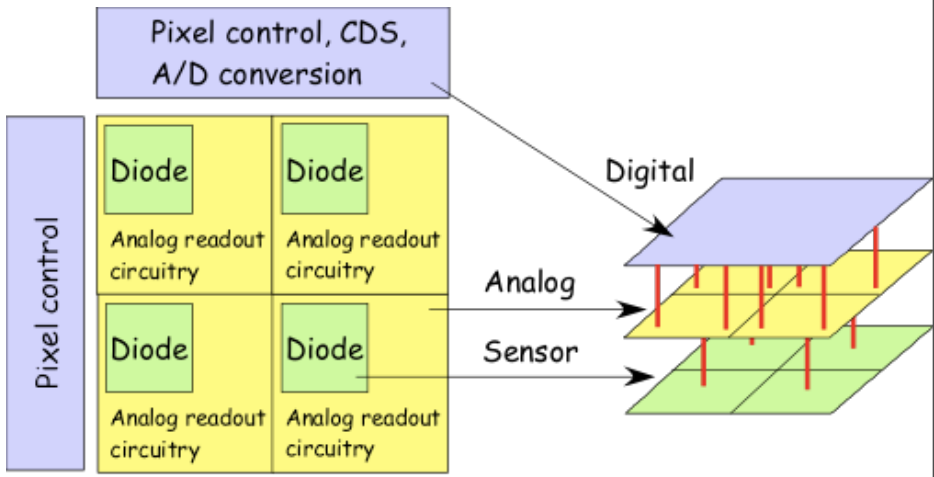
- SOI and 3D technologies can have very low node capacitance - $C_{pixel} < C_{strip}/n$ even with perimeter effects
- Can build high resolution low power high speed pixelated devices – if we are careful. Digital power may dominate in many applications.

3D Electronics Concept

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- Utilizes technology developed for Silicon-on-Insulator devices
- This is a major direction for the semiconductor industry.



Physicist's Dream



Conventional MAPS 4 Pixel Layout

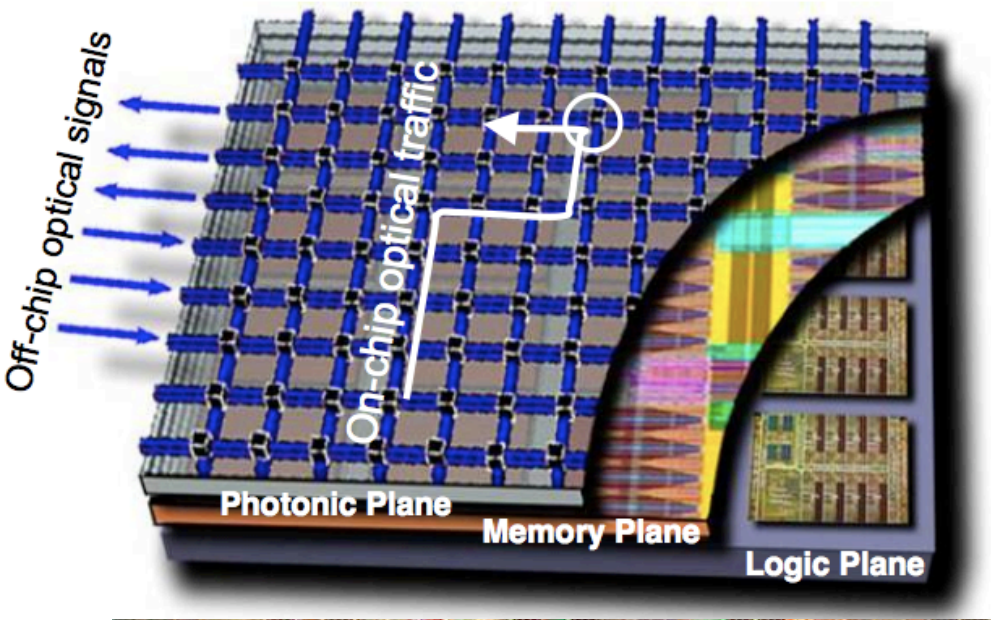
3D 4 Pixel Layout

Industry Initiatives

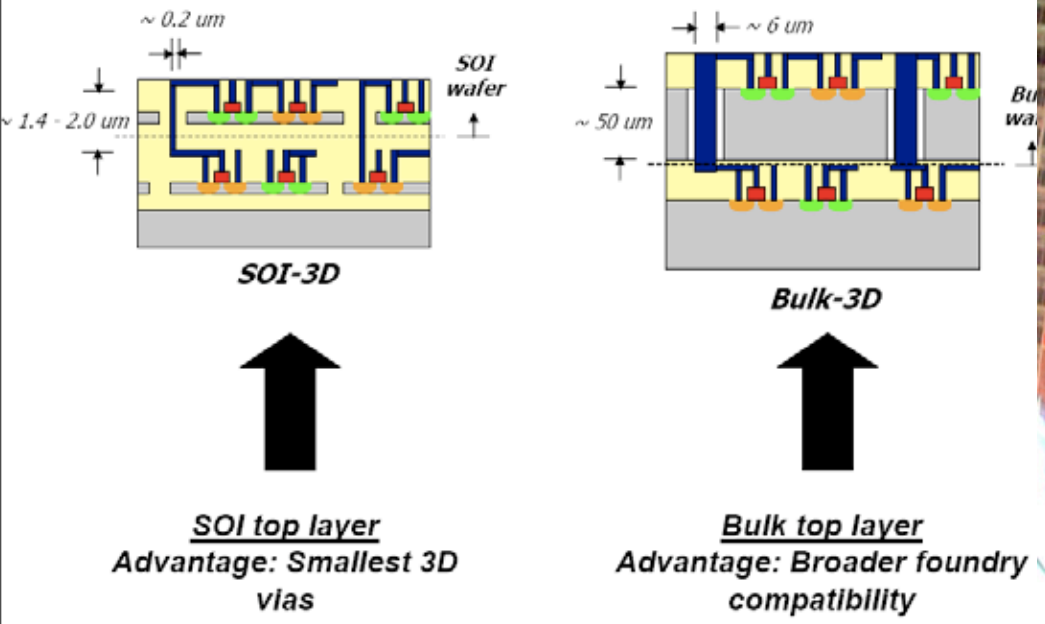
Yole Development report:

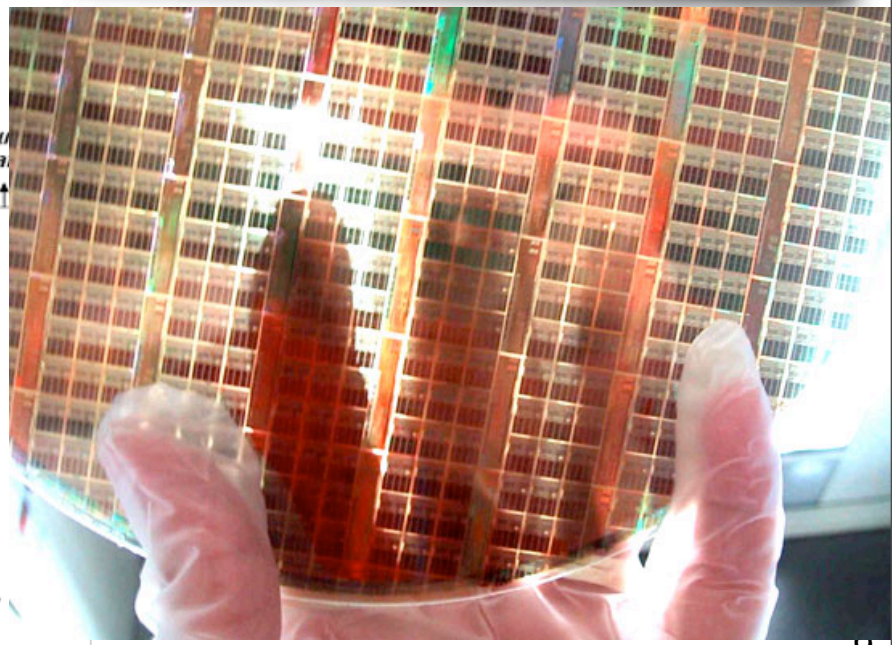
- 3D TSV packaging 2009 – total 750 K wafers. Wafer breakdown as follows:
  - 150mm wafers 145k (MEMS)
  - 200mm wafers 534k
  - 300 mm wafers 70k
- Current applications: MEMS, CMOS image sensors, Power amplifiers, Memories, High brightness leds
- Yole development has identified 15 pilot lines for 300 mm TSV process all around the world

IBM/Cornell/UCSB Study – vision of 22 nm 10Tflop 3D chip (2018)



Two Classes of 3DI Processes at I

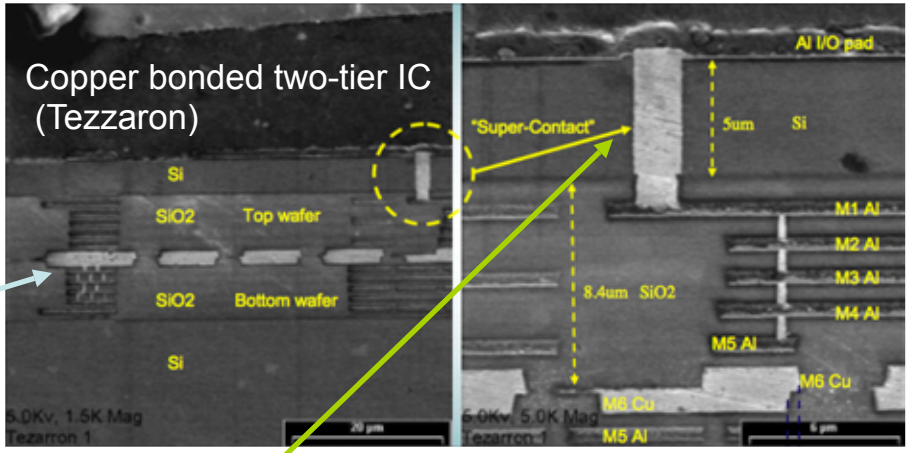


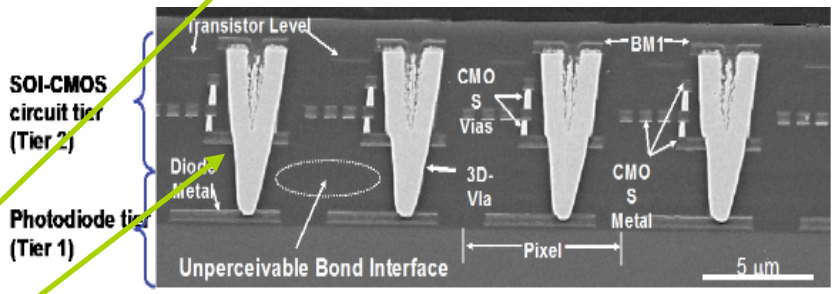


3D Ingredients

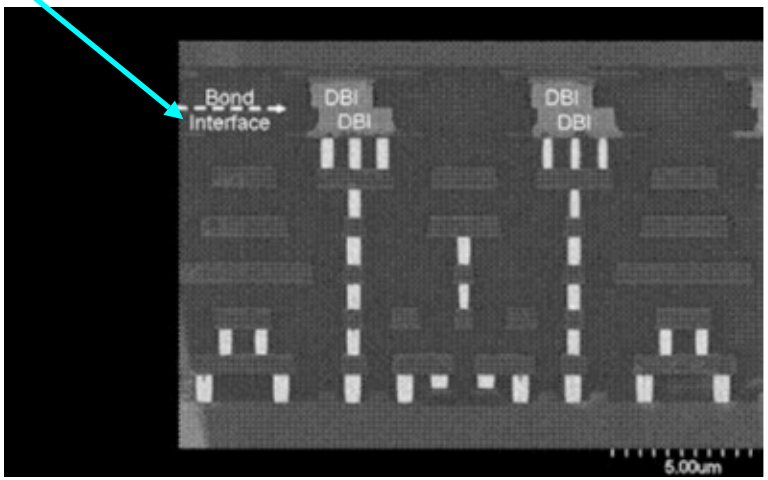
Technology based on:

1) Bonding between layers
   - Copper/copper
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation (SOI)
4) High precision alignment





8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)



8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

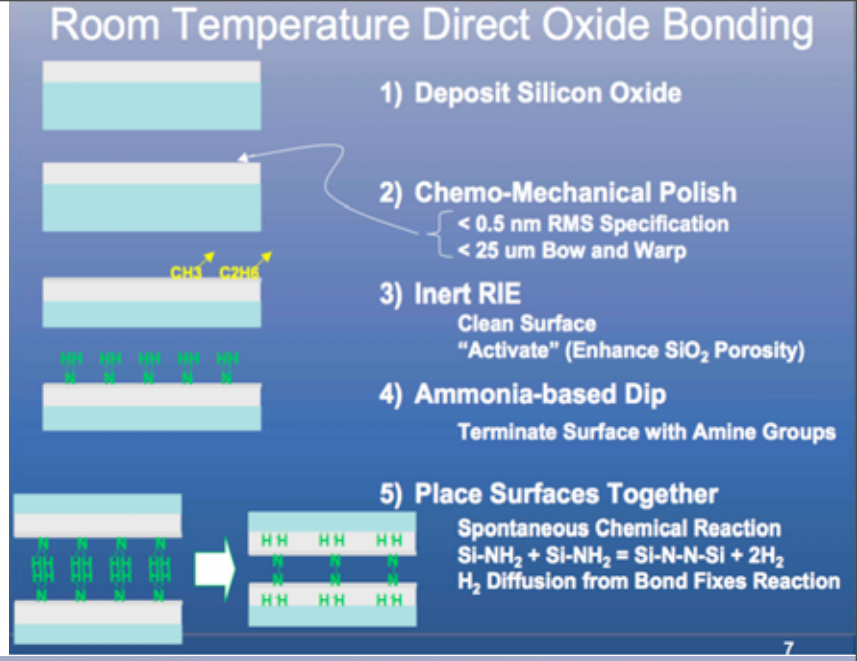
Fermilab Detector Initiatives

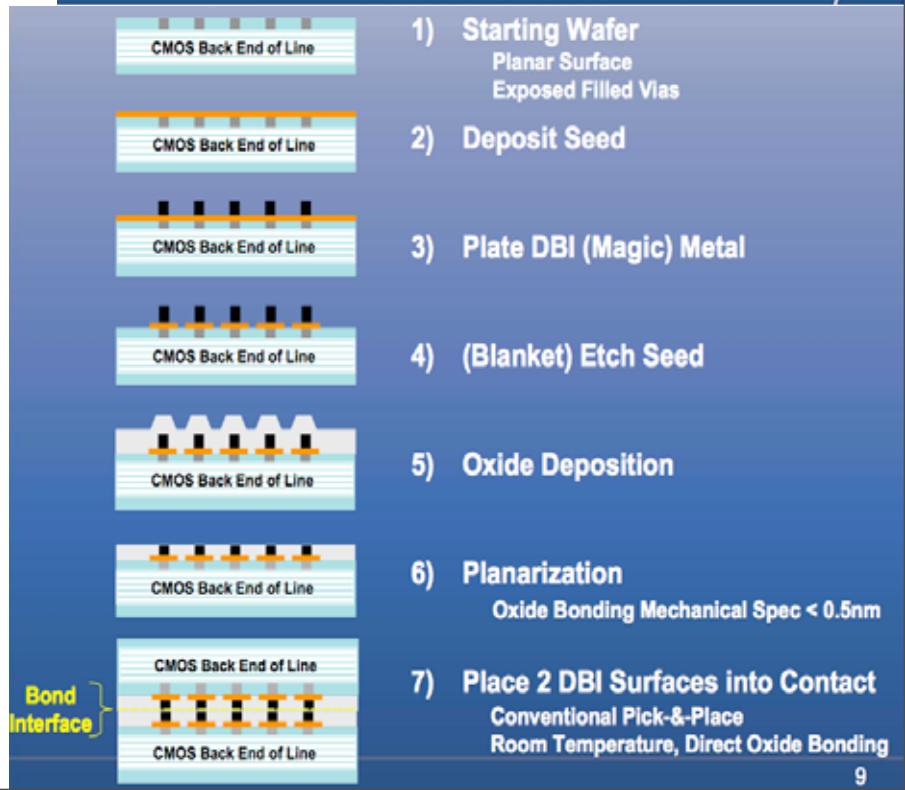
- VIP 3D chip for ILC
  - MIT-LL 3D SOI process
  - Tezzaron CMOS 3D process
- VIPIC chip for x-ray imaging
  - Tezzaron CMOS 3D process
- Thinned detectors
  - Laser annealing of the backside contact (with Cornell)
- Interconnections
  - DBI bonding of MIT-LL sensors with BTeV readout chip
  - Cu-Sn interconnects
- Silicon-on-insulator
  - Mambo imaging chip with KEK/OKI
  - American Semiconductor pixel R&D
- 3D multiproject run with Tezzaron

Applications to X-ray imaging, sLHC, lepton colliders

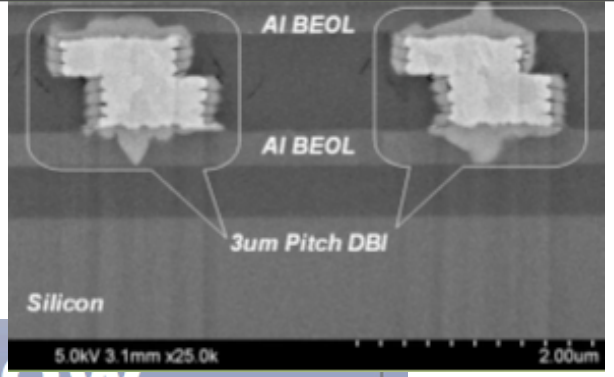
3D Integration by Oxide

- Ziptronix Direct Bonded Interconnect (DBI) based on formation of oxide bonds between activated SiO_2 surfaces with integrated metal
  - Silicon oxide/oxide inital bond at room temp. (strengthens with 350 deg cure)
  - Replaces bump bonding
  - Chip to wafer or wafer to wafer process
  - Creates a solid piece of material that allows bonded wafers to be aggressively thinned
  - ROICs can be placed onto sensor wafers with 10 µm gaps - full coverage detector planes
  - ROICs can be placed with automated pick and place machines before thermal processing - much simpler than the thermal cycle needed by solder bumps
- Process was developed to allow 3D integration of ICs by thinning to imbedded through silicon vias after bonding





DBI Process
(W. Bair, Ziptronix)



DBI™ Process Flow

Wafer Start (All Wafers)

Deposit Seed

Plate Metal

Etch Seed

Oxide Deposition

CMP

5 Steps

Dice Wafers (Upper Levels)

Ziptronix Bond Prep (Plasma + NH_4OH Dip)

Pick & Place

Bonding

Batch 350°C Anneal

Electrical Connections

Die Thinning

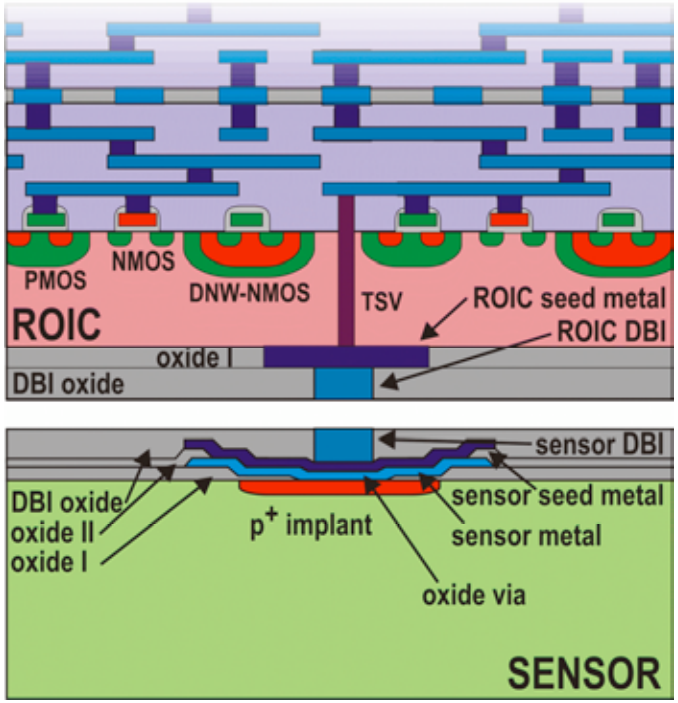
Optional

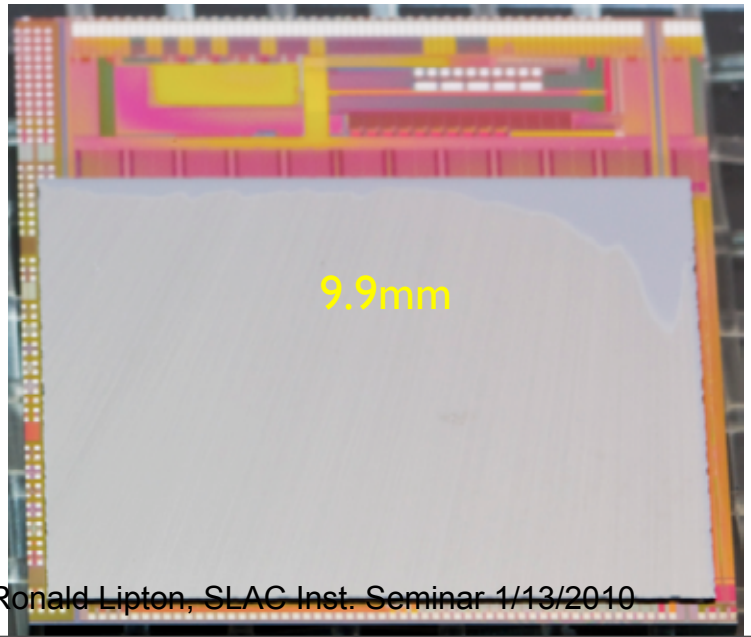
Conventional Unit Process

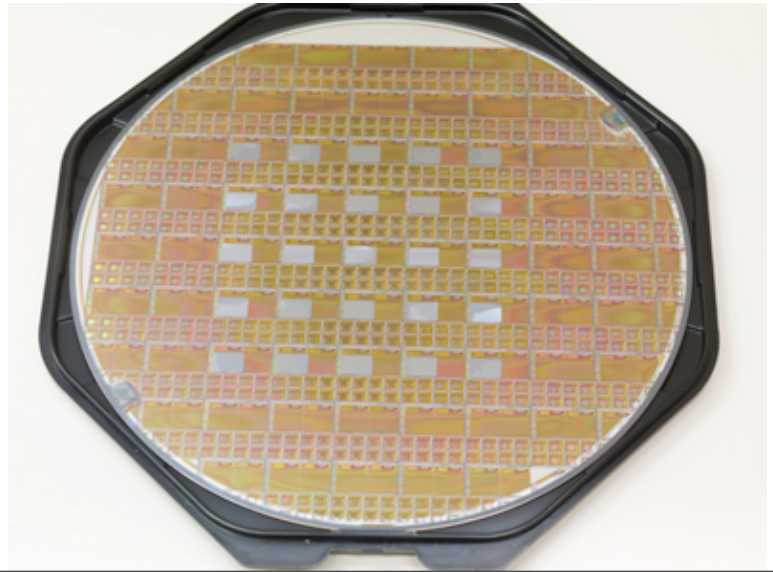
Ziptronix Unit Process

DBI Test Devices at FNAL

- Demonstration of technology with wafers we had "on hand"
  - BTeV FPiX 2.1 ROICs - 22 x 128 array of 50 x 400 micron pixels.
    0.25 micron TSMC CMOS - 8" wafers
  - MIT - LL 300 micron thick sensor wafers which had a matching pixel layout - 6" wafers
  - Sensor "chips" were bonded to 8" ROIC wafers, then thinned to 100 microns
  - Backside coated with In-Ga eutectic

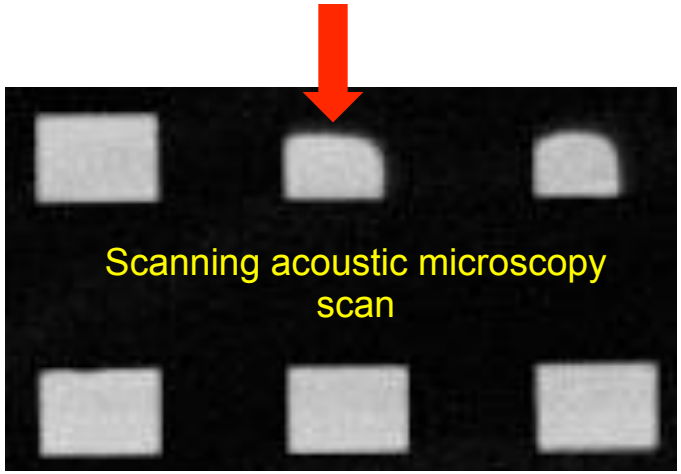




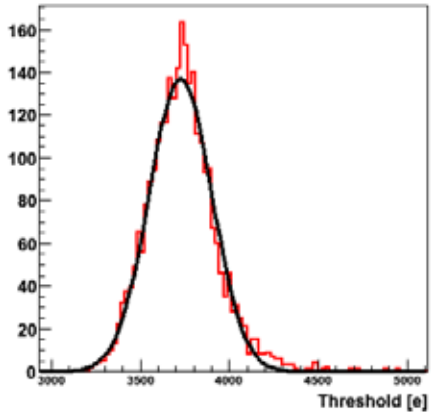


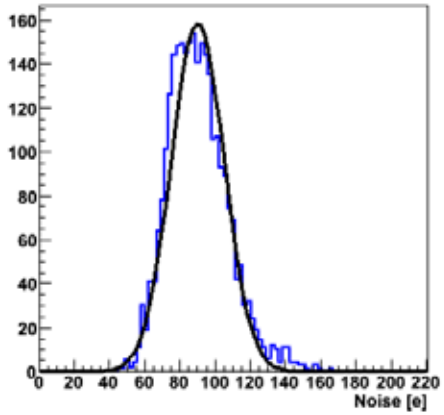
Bonded Device Tests

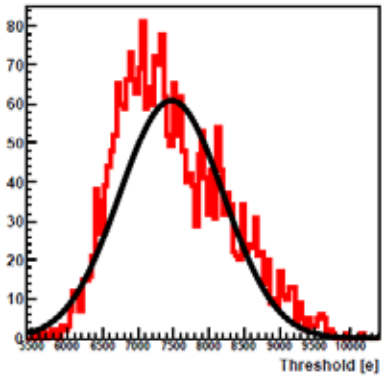
- FPIX2 has wrong polarity - designed to collect electrons - so dynamic range is degraded

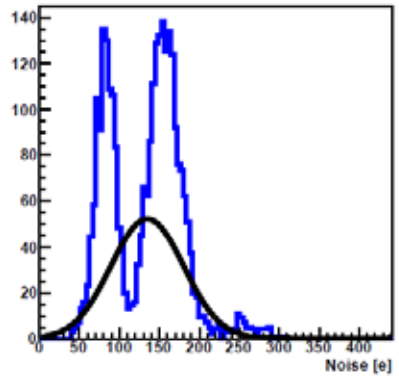


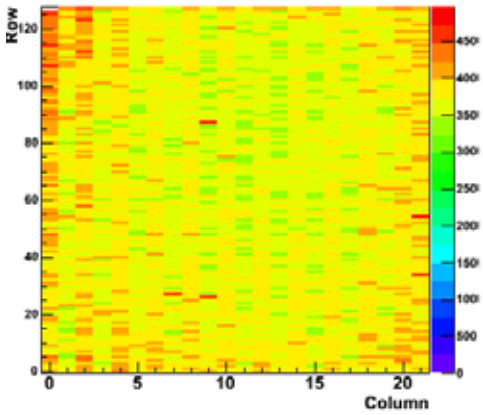
Example of a die with a void in the oxide bond

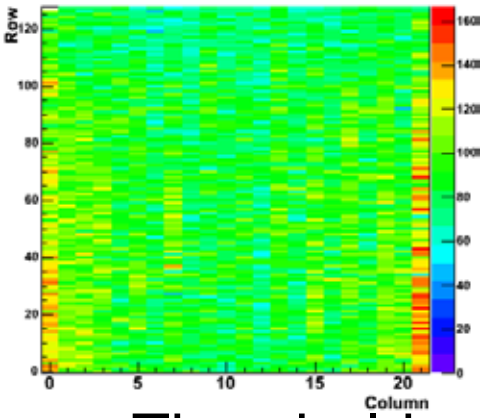


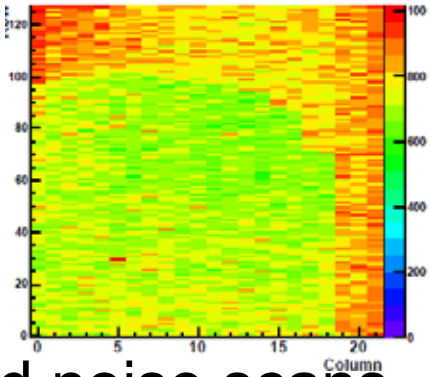


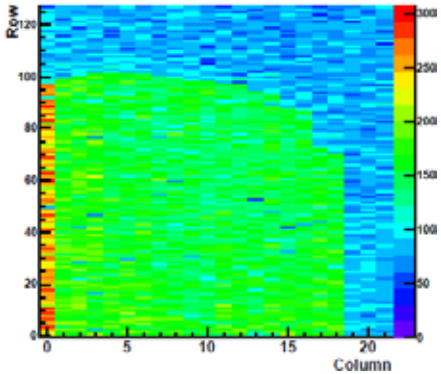








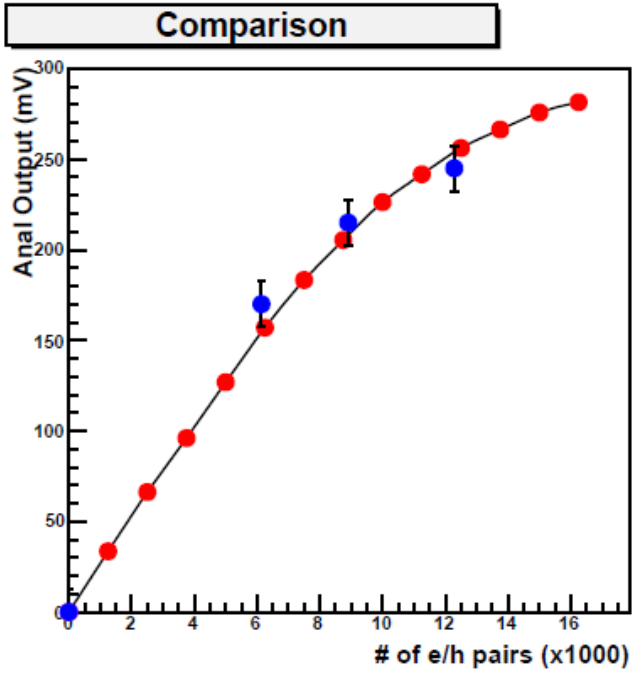


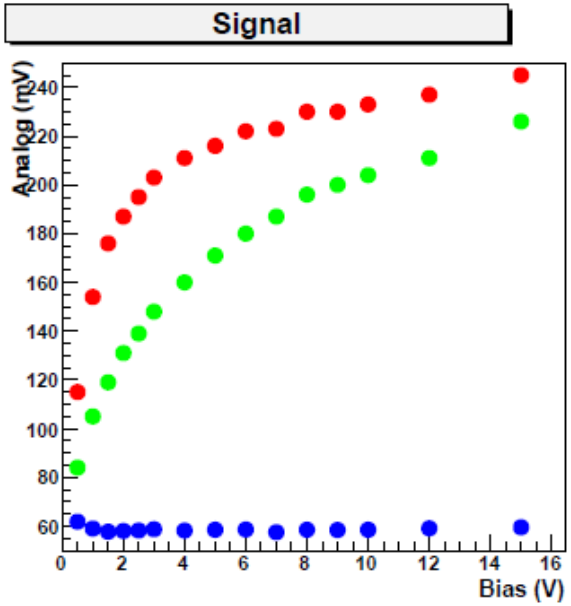


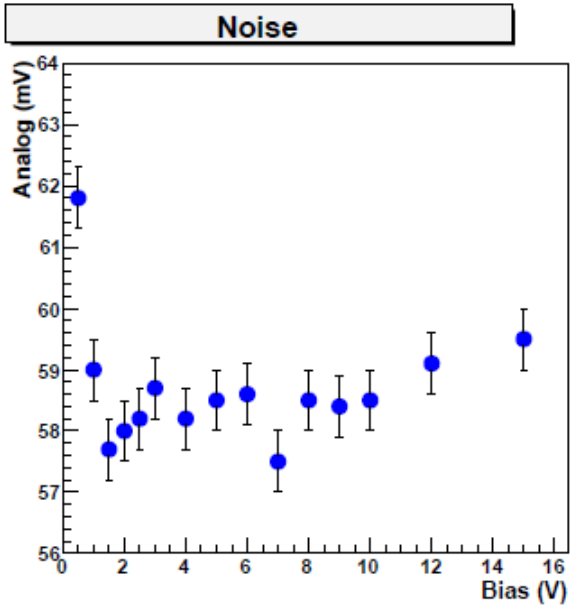
Threshold and noise scans

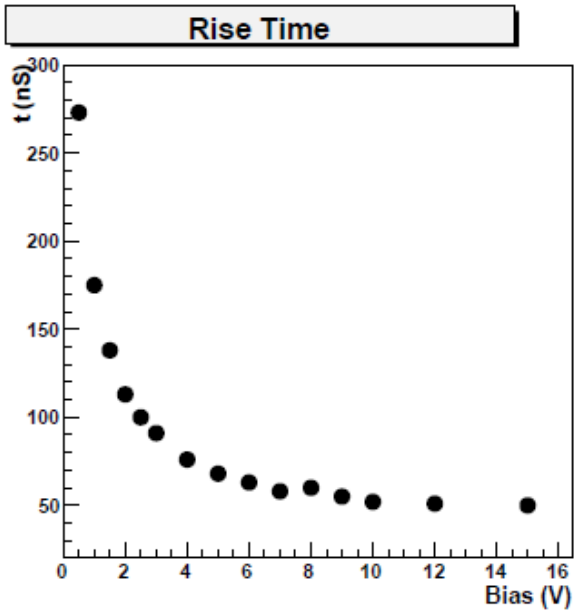
Laser and X ray tests

- 1064 nm laser used to test response of edge channels with analog outputs
  - $V_{depl} \sim 8V$
  - Low capacitance associated with interconnect
  - No evidence of digital to analog crosstalk
  - Good overall performance - all channels connected on die without bond voids.
  - Void rate ~ 4/21(wafer1), 12/25 (wafer 2)



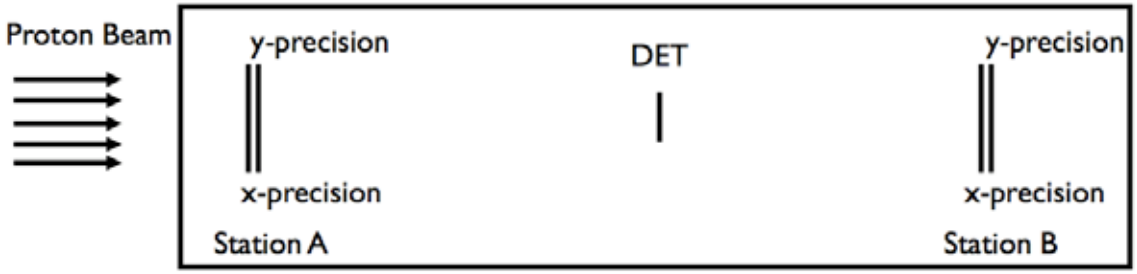


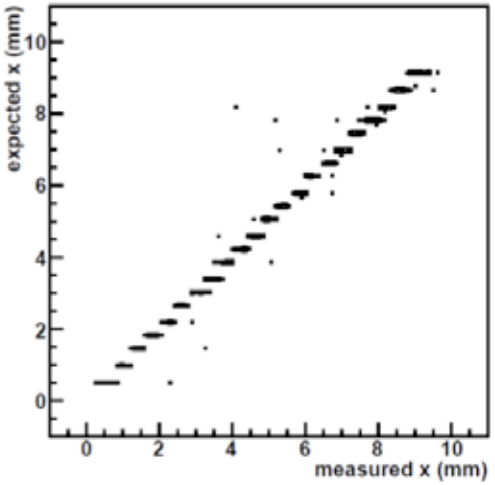


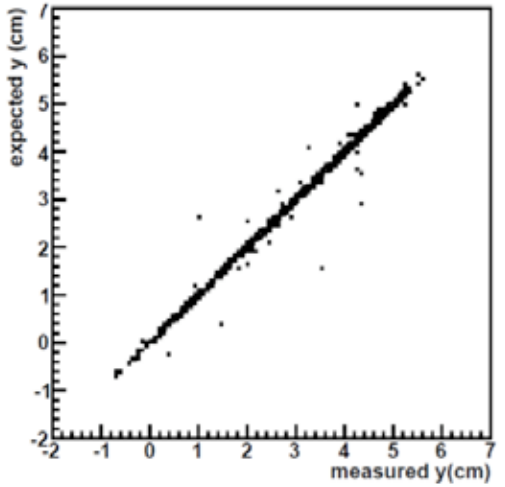


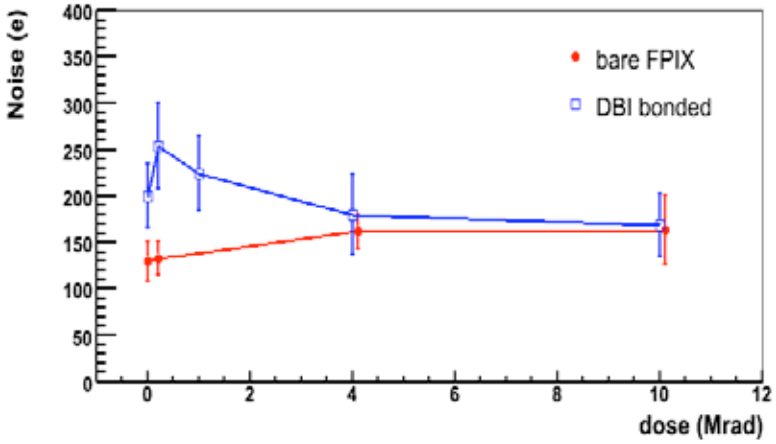
Beam and RadiationTests

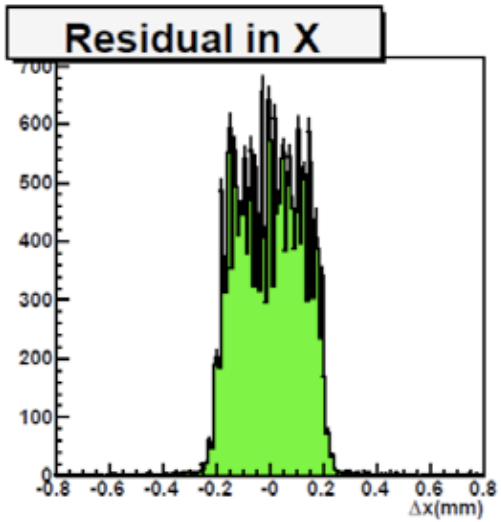
- FPIX telescope in the Fermilab Test beam with thinned sensors
- Good response and expected resolution.
- Recently performed a Co^{60} exposure to 10Mrad with no observed effects due to oxide bond

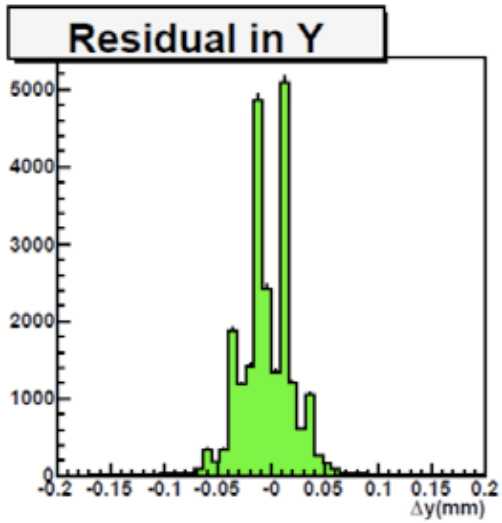










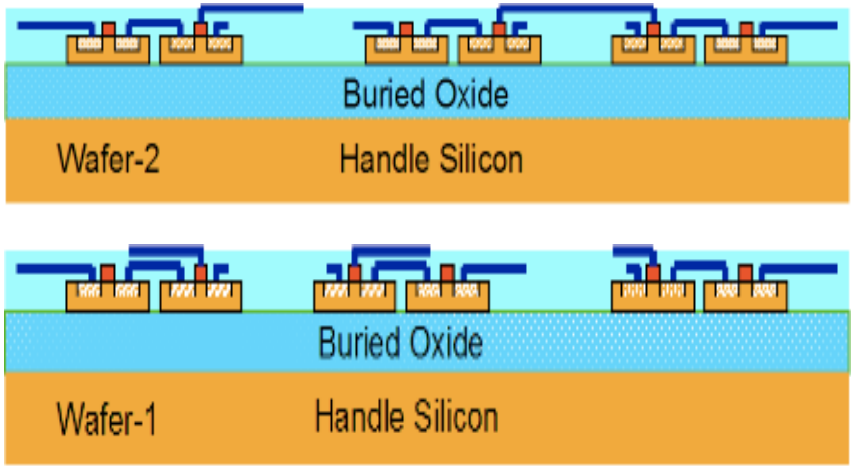


3D Pixel Design for ILC Vertex

- Goal - demonstrate ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel
- Previous technologies limited to very simple circuitry or large pixels
- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
- 3D density allows analog pulse height, sparse readout, high resolution time stamp in a 20 micron pitch pixel.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
  - 64 x 64 pixel demonstrator version of 1k x 1k array.
  - Submitted to 3 tier DARPA-sponsored multi project runs. Sensor to be added later.
- Low power front end 1875 $\mu W/mm^2$ x Duty Factor

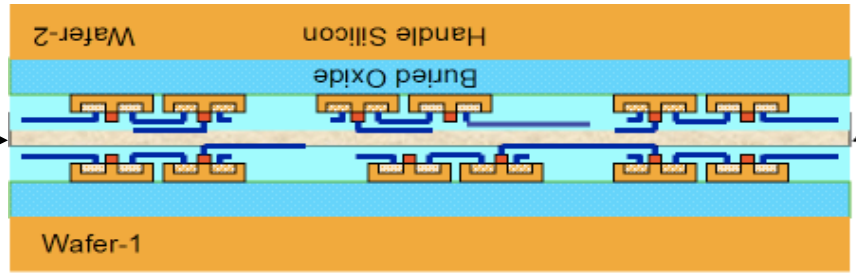
- 3 tier chip
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers



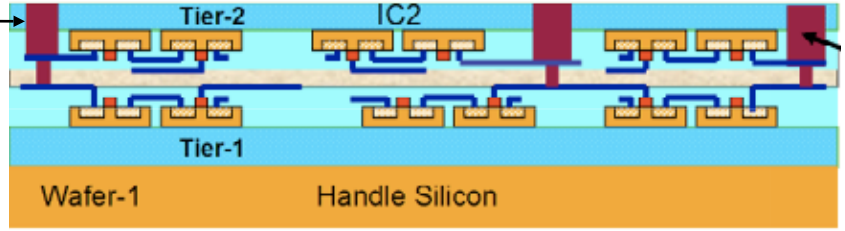
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

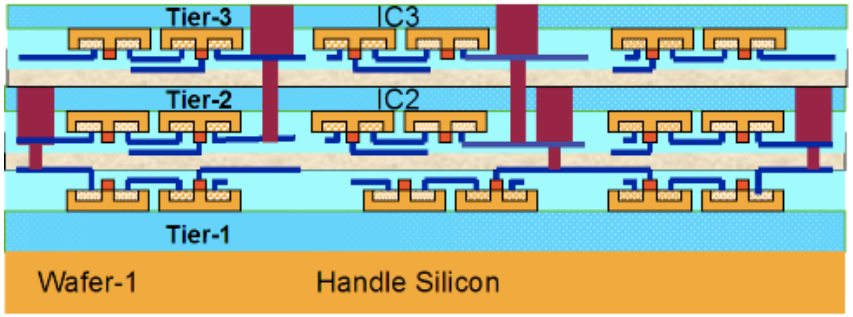


3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via

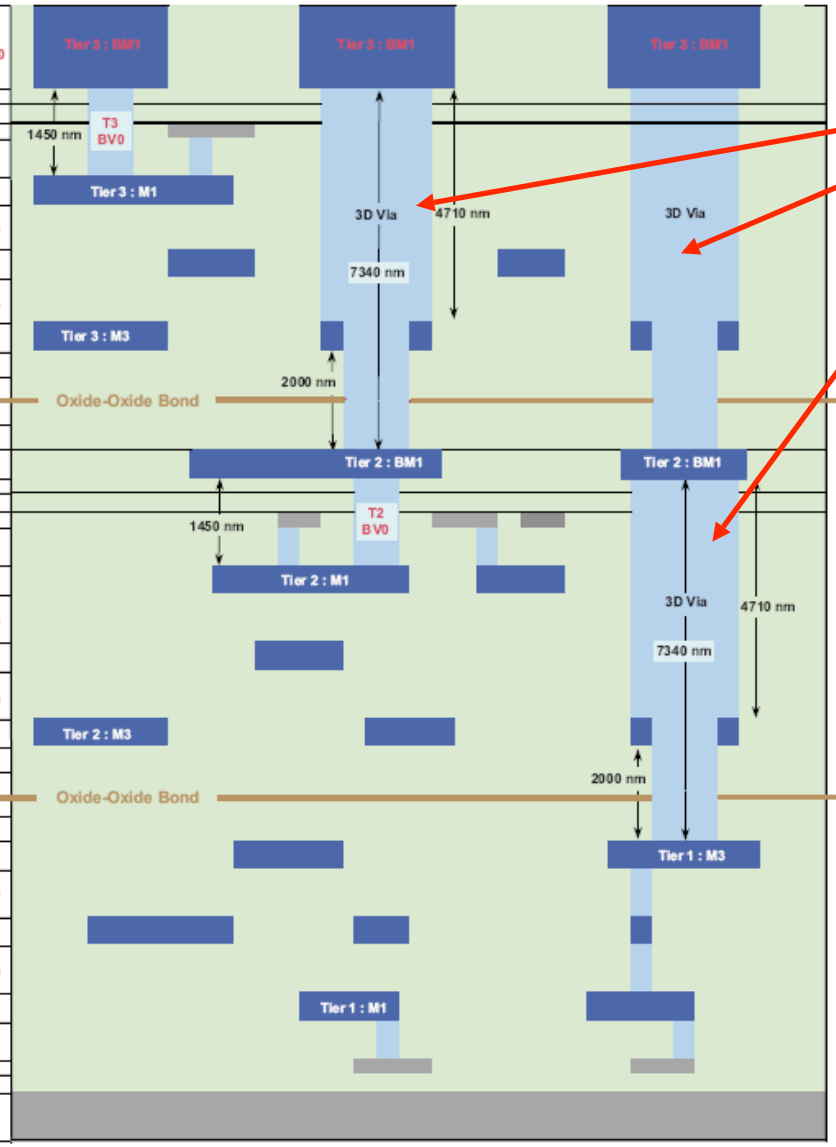


4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



MIT-LL 3D Multiproject Run Chip Cross Section

Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	



3D vias

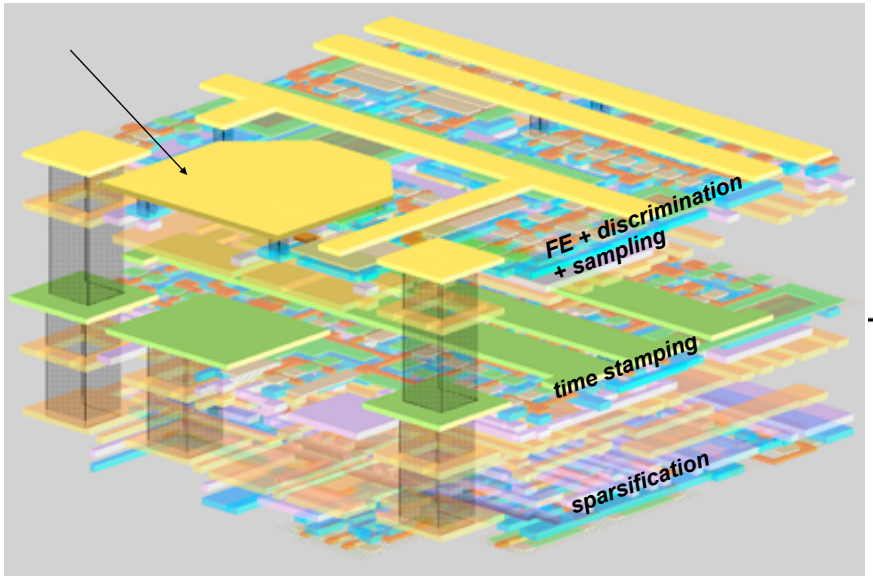
8.2 μm

7.8 μm

6.0 μm

Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

3D Geometry

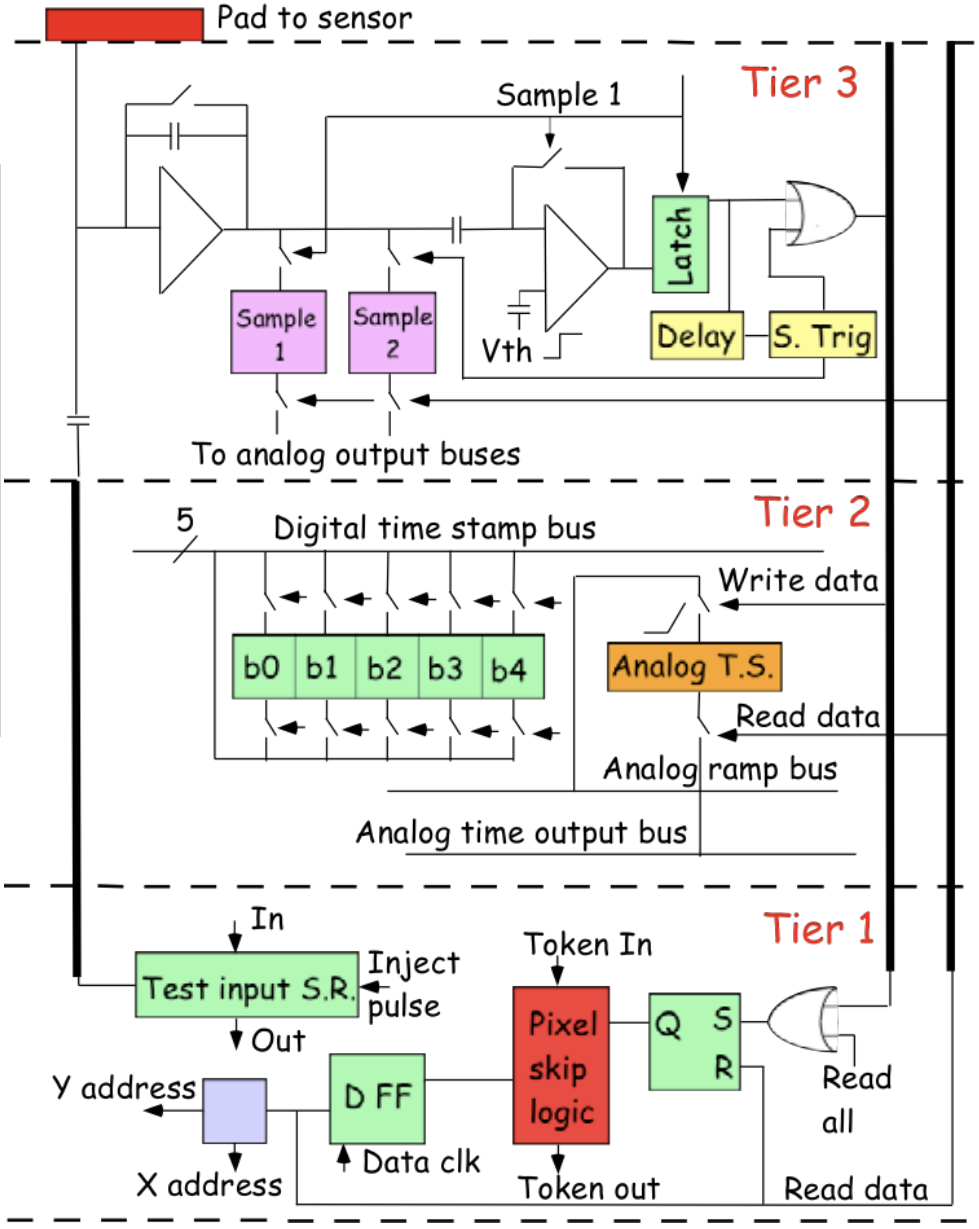


Chip designers:

Tom Zimmerman

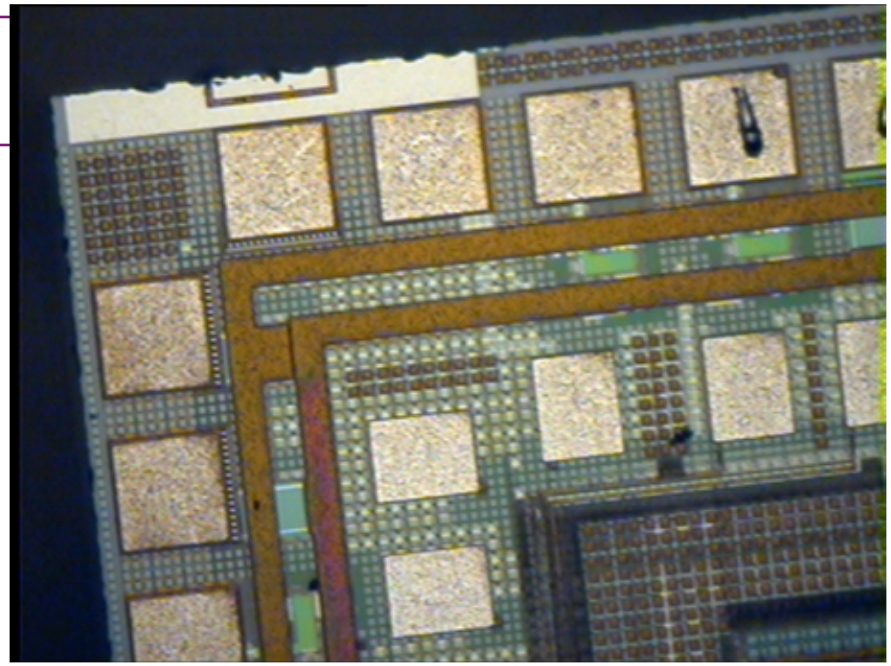
Gregory Deptuch

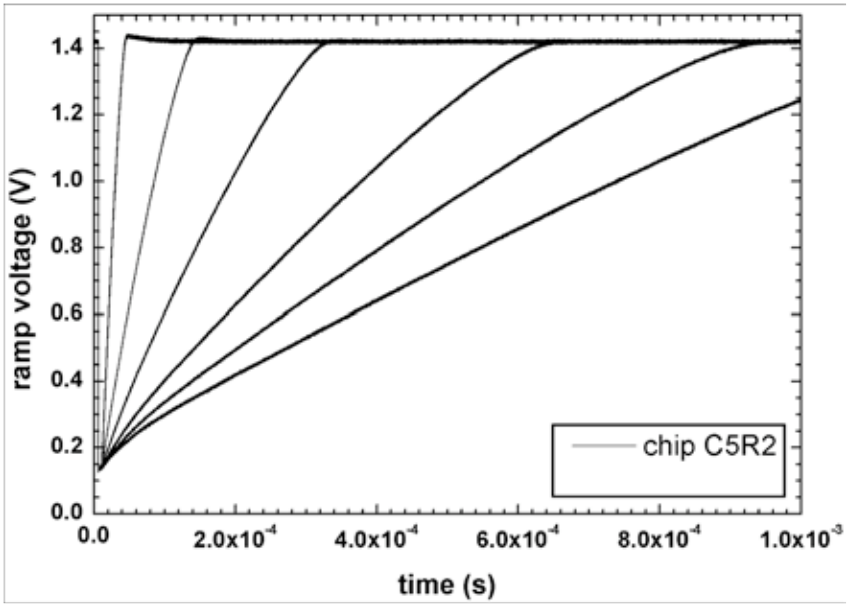
Jim Hoff



VIP1 Test Results

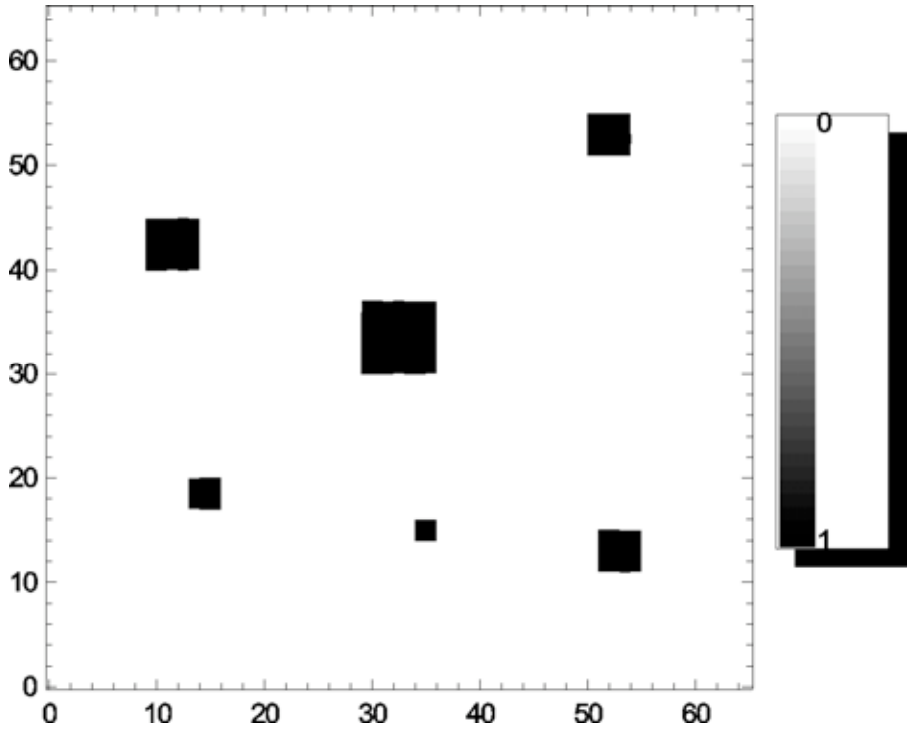
- Basic functionality of the chip was demonstrated
  - Propagation of readout token
  - Threshold scan
  - Input test charge scan
  - Digital and analog time stamping
  - Full sparsified data readout
- No problems could be found associated with the 3D vias between tiers.
- Chip performance compromised by SOI issues:
  - Large leakage currents in transistors and diodes
  - Poor current mirror matching, Vdd sensitivity, low yield
- An improved version of the VIP was submitted to MIT LL in October 2008. The new chip is called VIP2
  - More conservative design, larger features - less dependence on dynamic logic, pixel size 20->30 micron

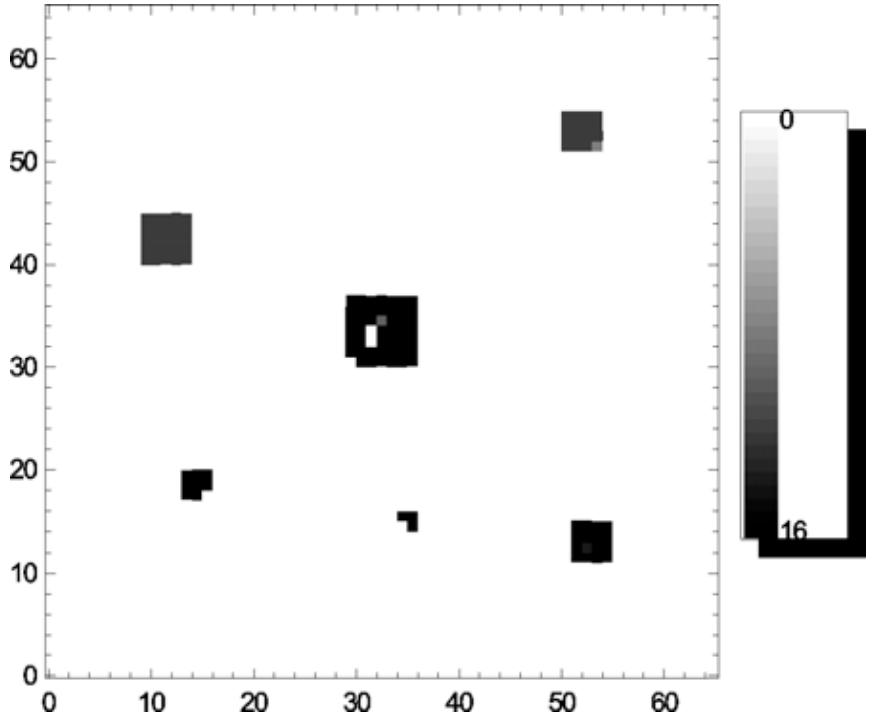




VIP1 Full Array Sparse Readout

Injection of Test Charge into 119 Integrator Inputs of 64 x 64 Array





Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal

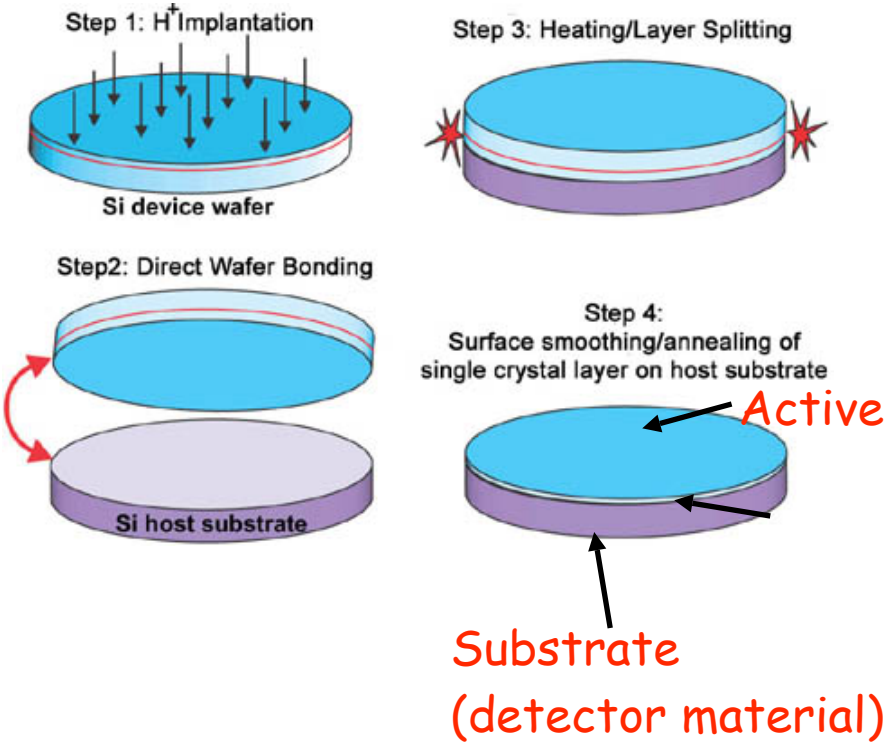
Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

23

Silicon on Insulator

- SOI is based on a thin active circuit layer on an insulating substrate. Modern technology utilizes ~200 nm of silicon on a "buried" oxide (BOX) which is carried on a "handle" wafer.
- *The handle wafer can be high quality, detector grade silicon, which opens the possibility of integration of electronics and fully depleted detectors in a single wafer with very fine pitch and little additional processing.*
- Diode can be formed by implantation through the BOX
- Used for high speed, circuits, immune to SEU
- Important for 3D integration

(Soitech illustration)

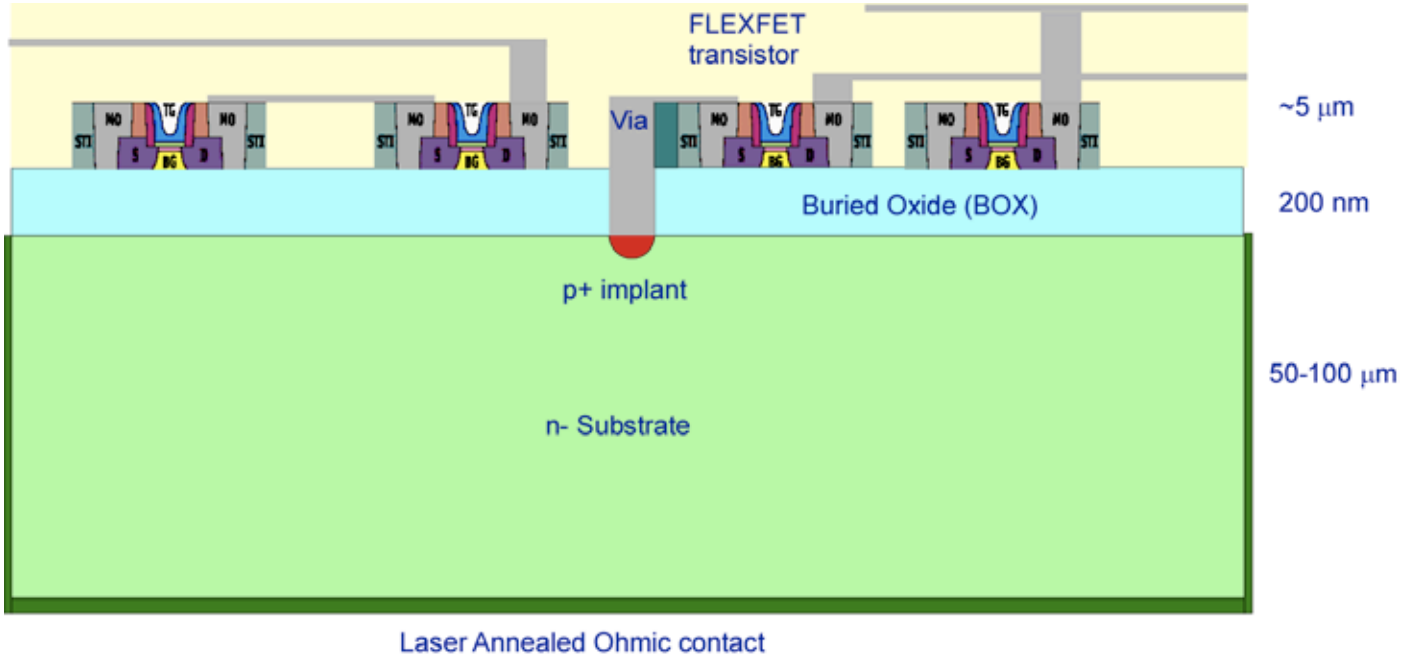


Steps for SOI wafer formation

SOI Detector for HEP

not to scale

Minimal interconnects,
low node capacitance

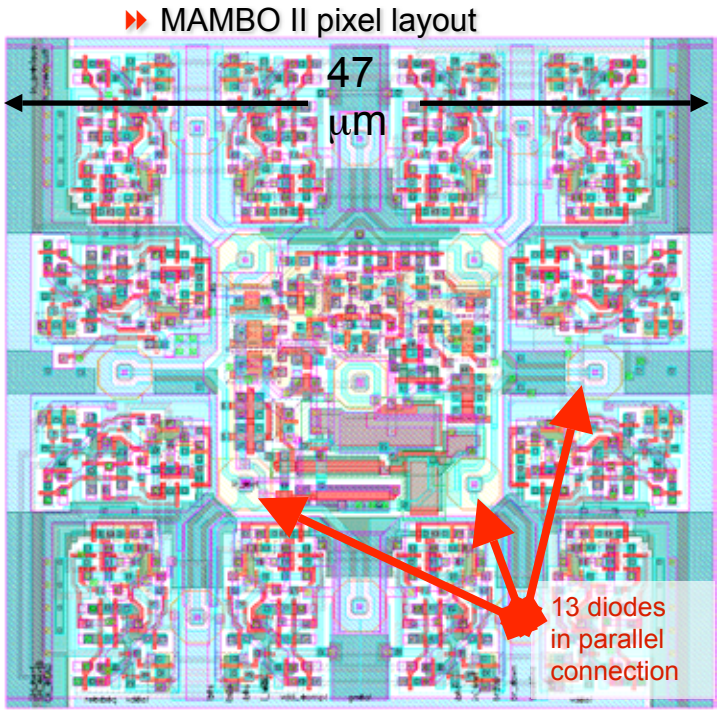


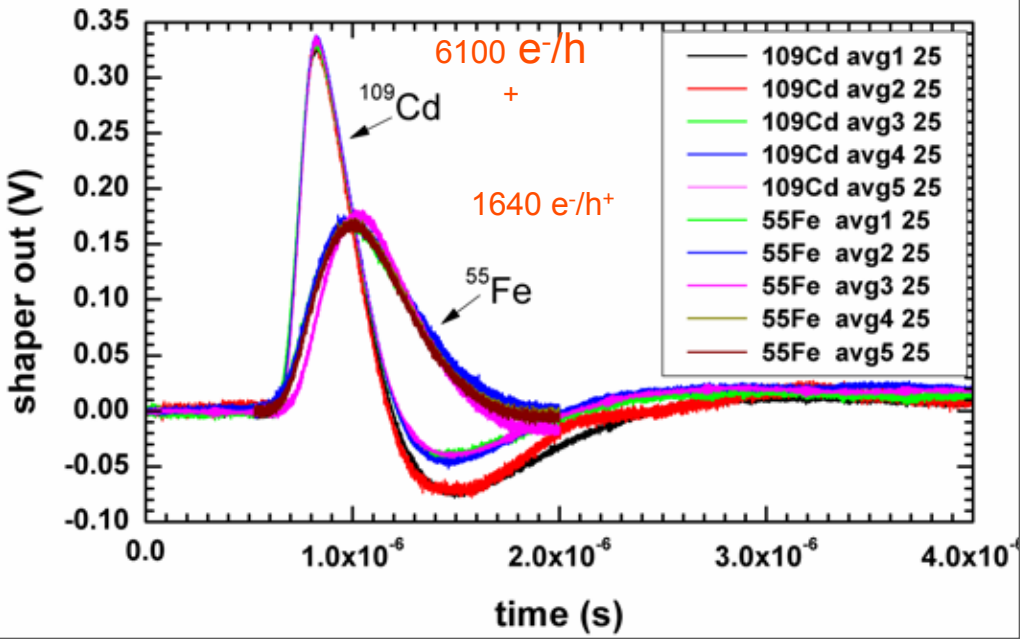
High resistivity
Silicon wafer,
Thinned to 50-
100 microns

Backside implanted after thinning
Before frontside wafer processing
Or laser annealed after processing

SOI R&D

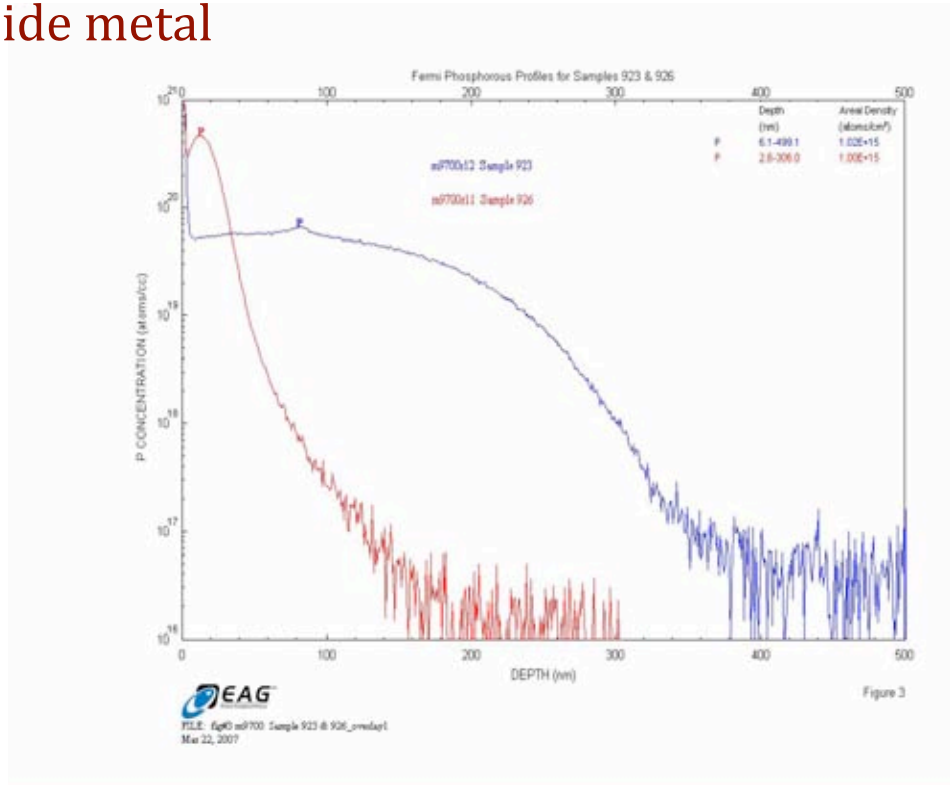
- KEK sponsored multiproject run at OKI. The chip incorporates a 12 bit counter array for a high dynamic range x-ray or electron microscope imaging.(G. Deptuch)
- Counting pixel detector plus readout circuit
  - Maximum counting rate ~ 1 MHz
  - Each pixel: CSA, CR-RC2 shaper, discriminator + 12 bit binary counter
- Max implant pitch (4/pixel) is determined by the "back gate" effect where the topside transistors thresholds are shifted by handle potential





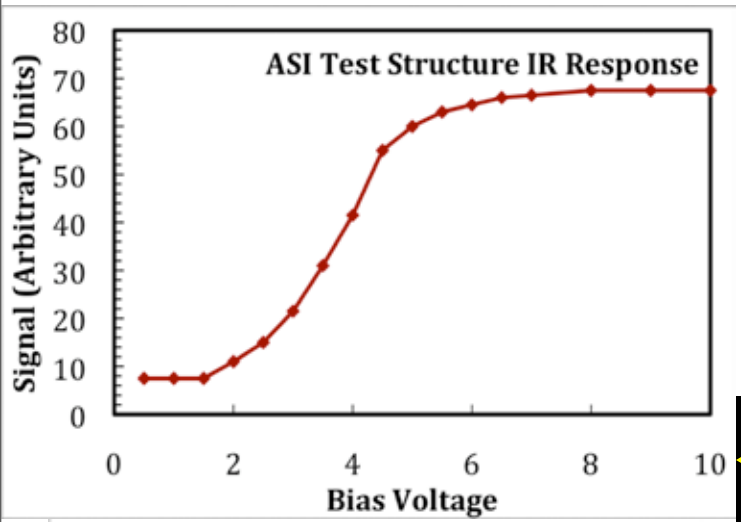
Thinning and Laser Annealing

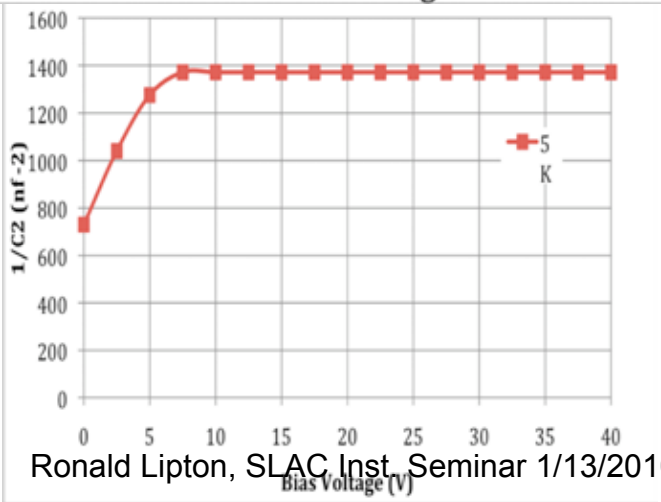
- To be useable for HEP the SOI detectors need to be thinned – any of several processes can be used.
- We need to provide a backside ohmic contact to the thinned wafer.
  - Normally done by ion implantation activated using furnace anneal at ~1000 deg C.
  - But the topside has been fully processed and we need to keep the top below ~500 deg C to protect topside metal
- Use a raster scanned eximer laser to melt the silicon backside locally – this activates the ohmic implant and repairs the implantation damage by recrystallizing the silicon
- Done for Micron, MIT and American Semiconductor test wafers



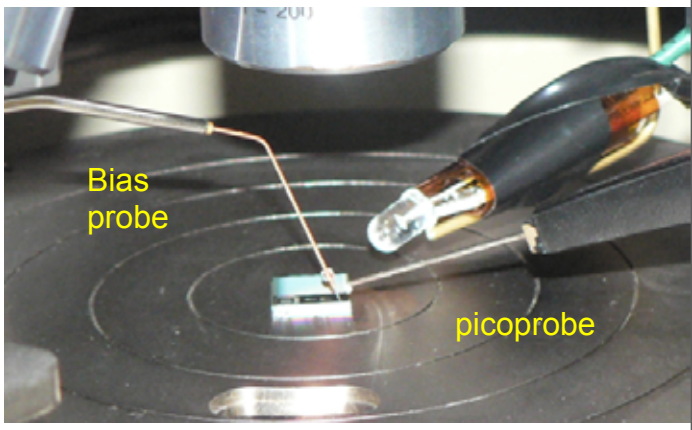
SOI Sensors

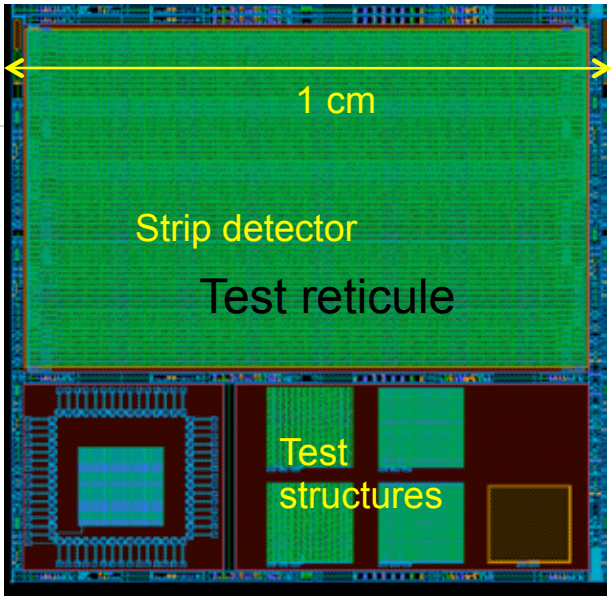
- American Semiconductor dual gated FLEXFET – avoids backgate effect
- Thinned to 50 microns, ion implanted, laser annealed at Cornell University
- Sensors only fabricated on handle wafer

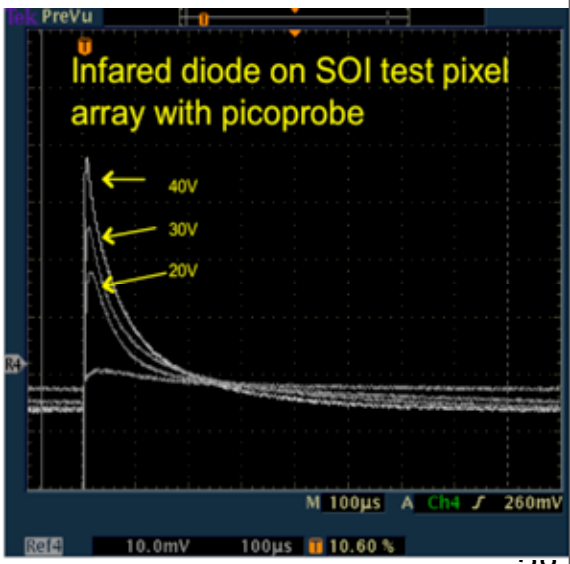




Signals measured directly using Pico probe and 1060nm diode





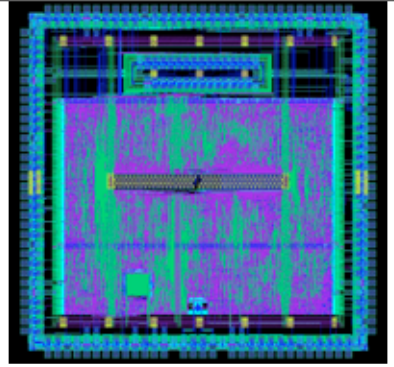


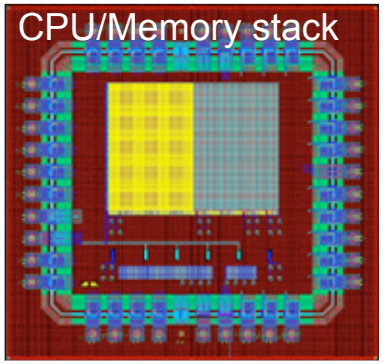
Commercial 3D Bonding

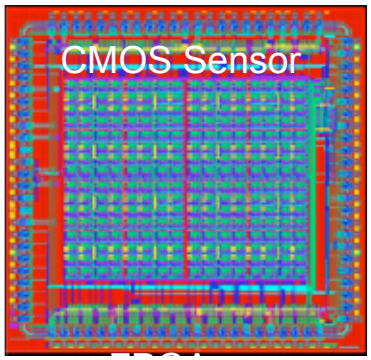
- There are 3 vendors that have commercially available (external) 3D processes.
  - Tezzaron – uses CuCu thermocompression for bonding
  - Ziptronix- uses Direct Bond Interconnect (oxide bonding)
  - Zycube – uses adhesive and In-Au bumps for bonding
- Fermilab is working with Tezzaron to fabricate 3D integrated circuits using CuCu bonding.
- Others developing CuCu bonding include IBM, RPI, MIT
- Fermilab is working with Ziptronix to do low mass bonding with DBI to detectors. (FPIX chips to 50 um thick sensors.)
- KEK is working with Zycube

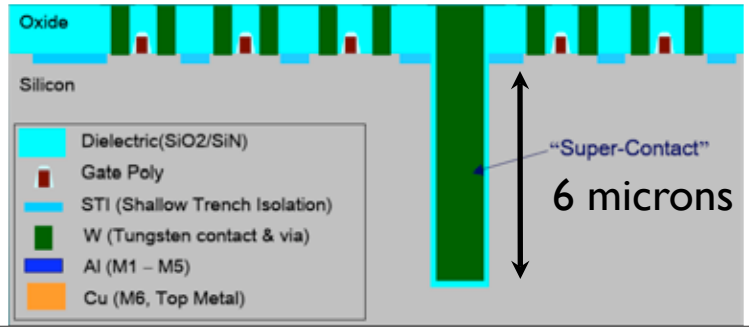
Tezzaron 3D Process

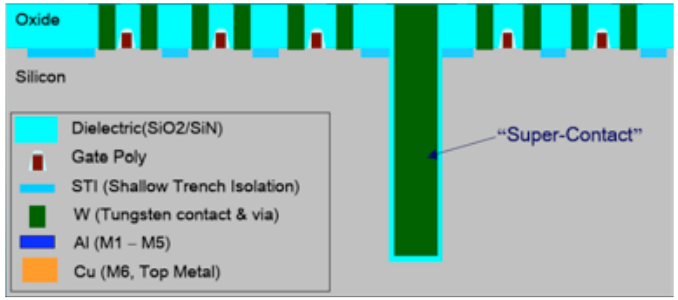
- Tezzaron (Naperville) has developed a 3D process utilizing CMOS wafers from a commercial IC foundry with cu-cu bonding and "standard" thinning and lith.
- Wafers with "vias first" are made as a process option at Chartered Semiconductor in Singapore.
- Wafers are bonded, thinned and topside processed in Singapore by Tezzaron
  - Bond pads
  - Bump bond pads
- Commercial (10^6 8" wafers), well characterized 0.13 micron process - avoids issues seen with MIT/OKI
- Bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 um
  - Missing bond connections = 0.1 PPM



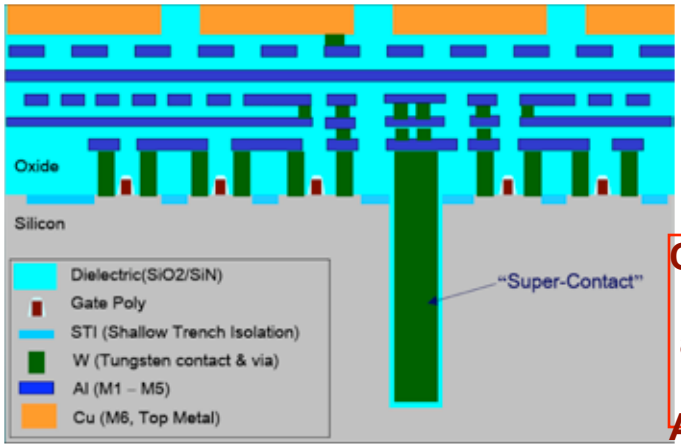






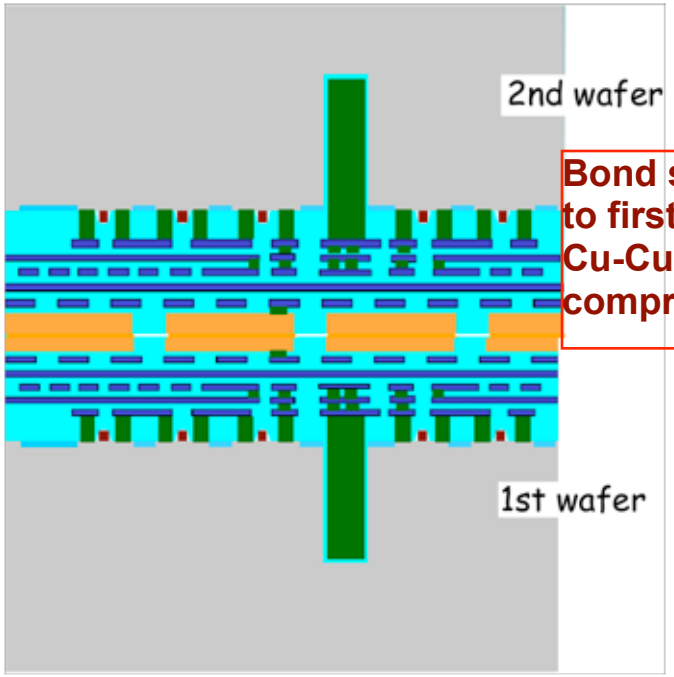


Transistor fabrication
Form supercontact
Fill supercontact



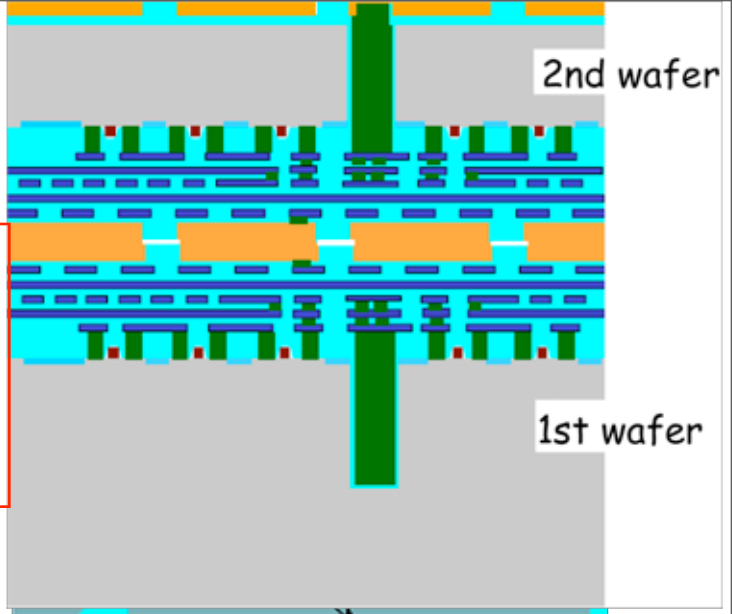
Thin the second wafer to about 12 um to expose contact.
Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd

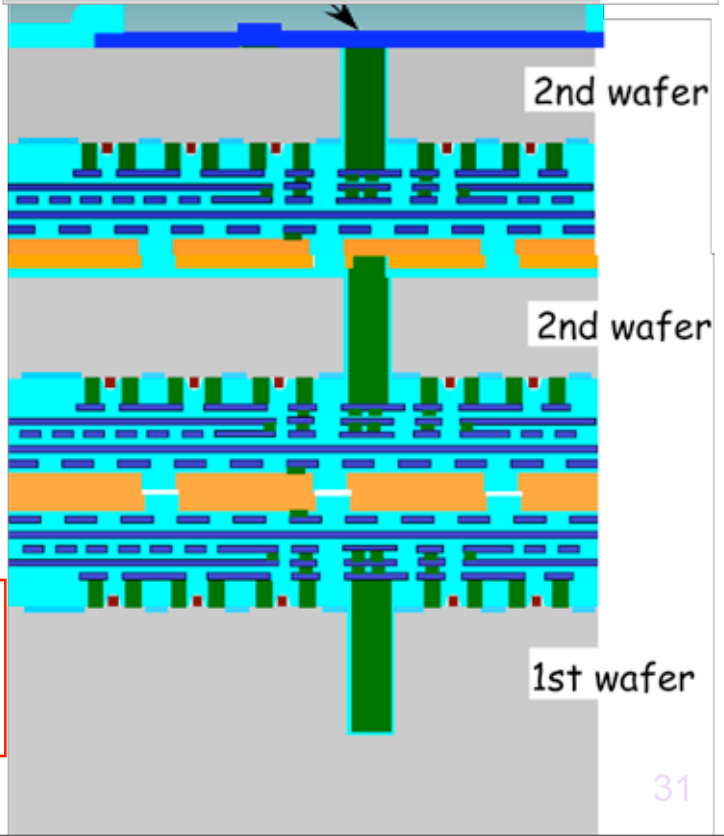
Complete back end of line processing by adding Cu metal layers
And top Cu metal

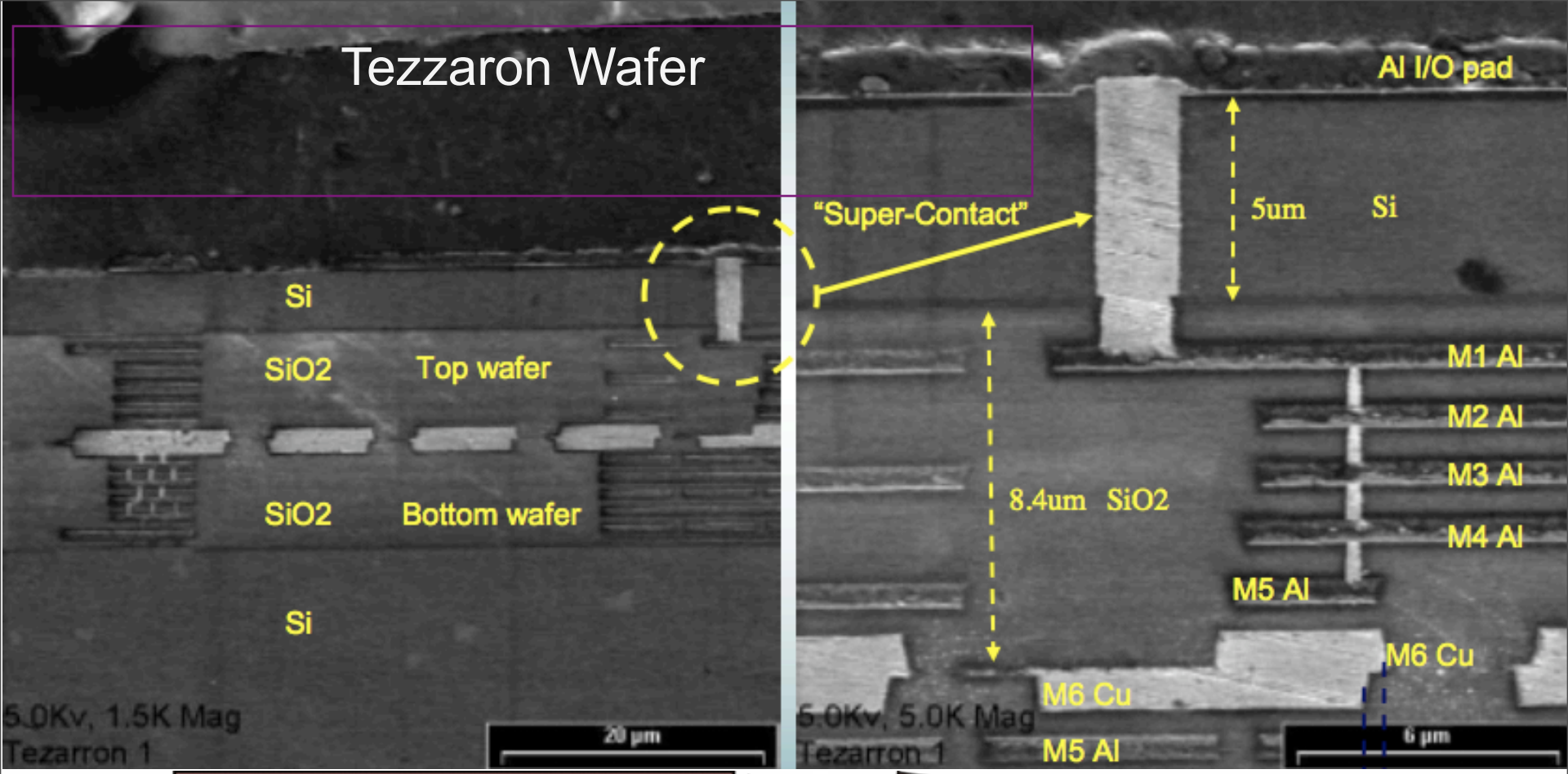


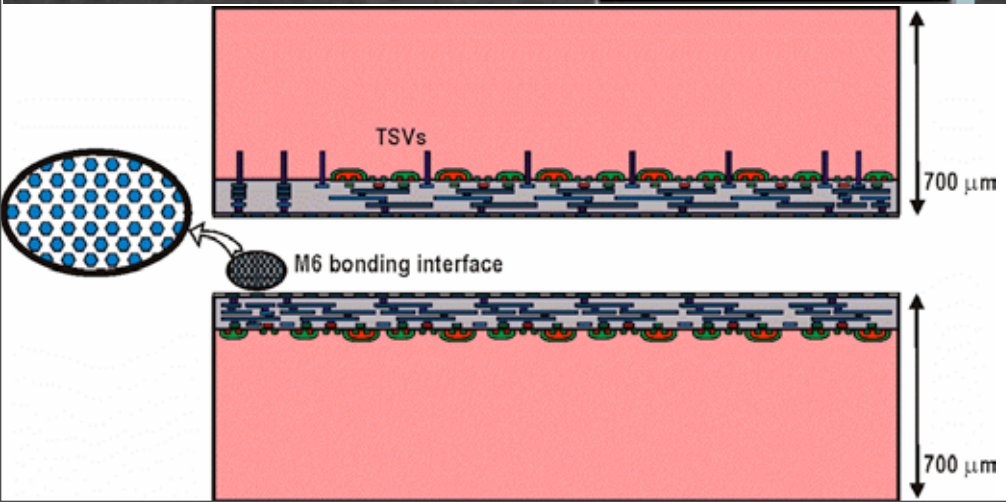
Bond second wafer to first wafer using Cu-Cu thermo-compression bond

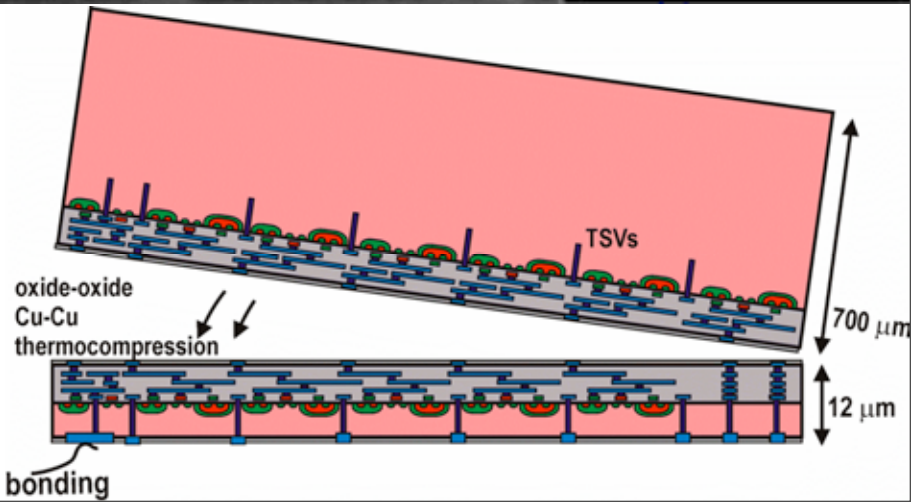
Stack 3rd waferThin 3rd wafer Add final Passivation and metal for bond pads



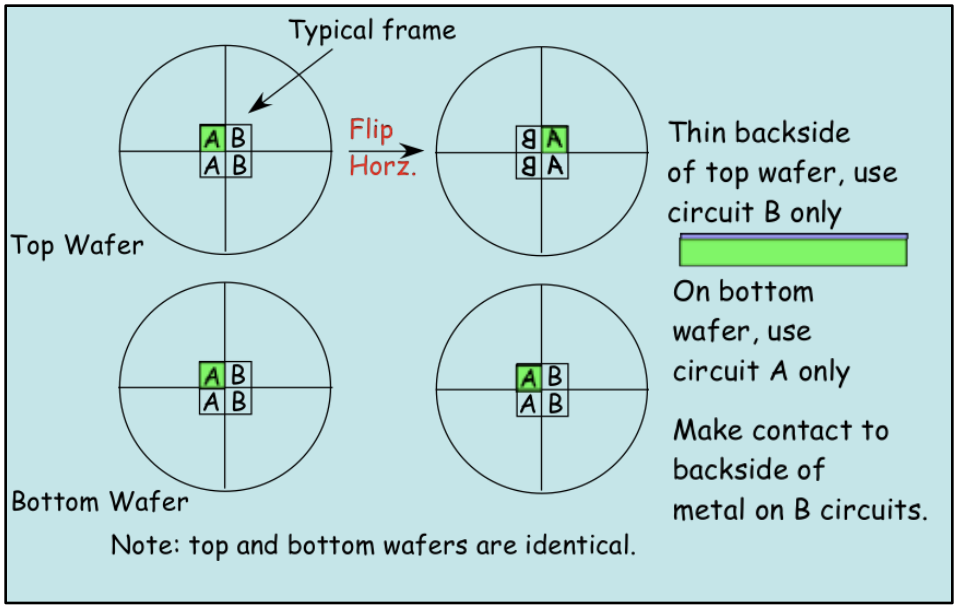



Tezzaron Wafer
Si
SiO2
Top wafer
SiO2
Bottom wafer
Si
5.0Kv, 1.5K Mag
Tezzaron 1
20 µm
Al I/O pad
"Super-Contact"
5um
Si
M1 Al
M2 Al
M3 Al
M4 Al
M5 Al
M6 Cu
8.4um SiO2
M6 Cu
M5 Al
5.0Kv, 5.0K Mag
Tezzaron 1
6 µm


TSVs
700 µm
M6 bonding interface
700 µm


TSVs
700 µm
oxide-oxide
Cu-Cu
thermocompression
12 µm
bonding

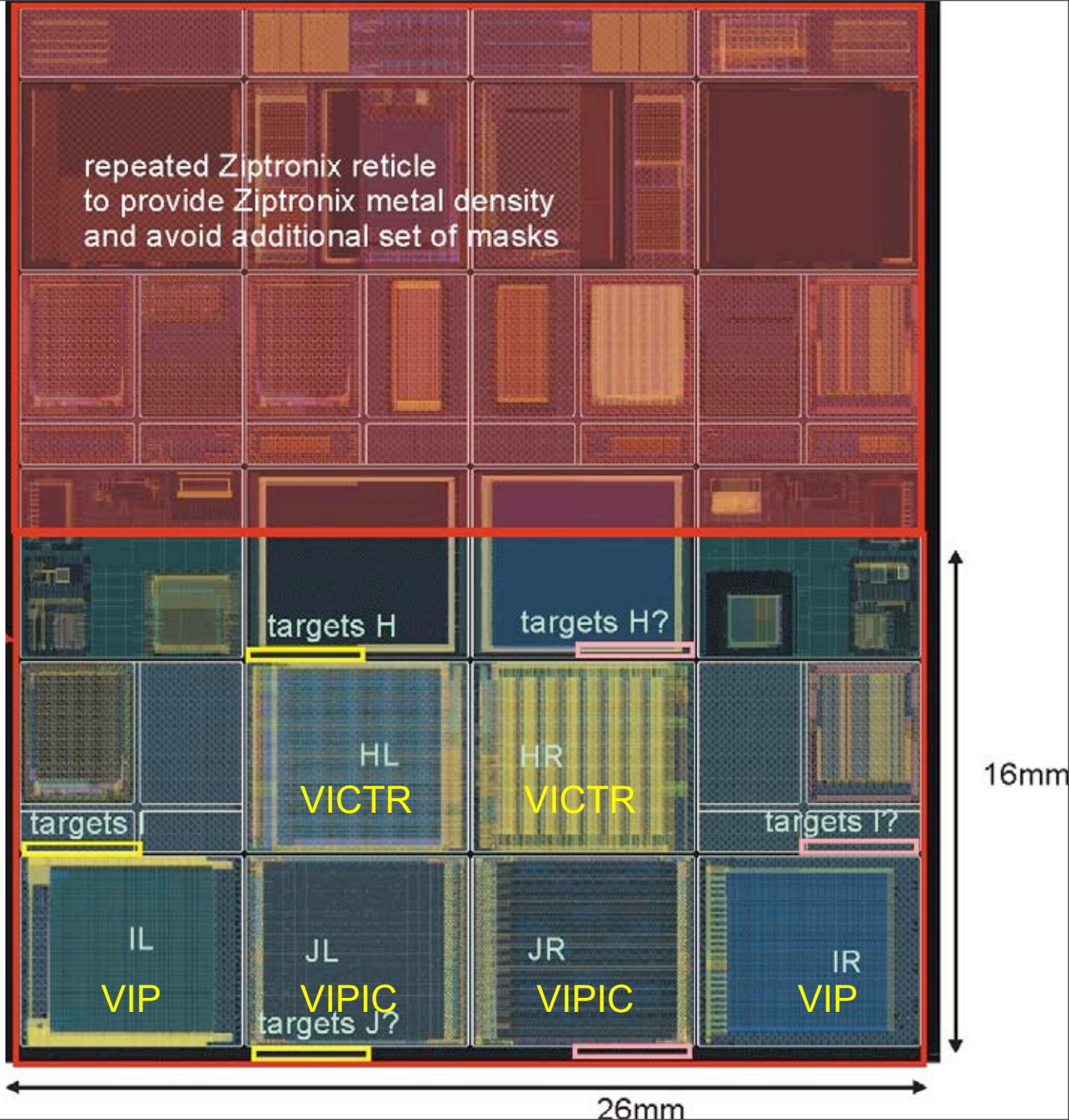
Fermilab Tezzaron Multiproject Run

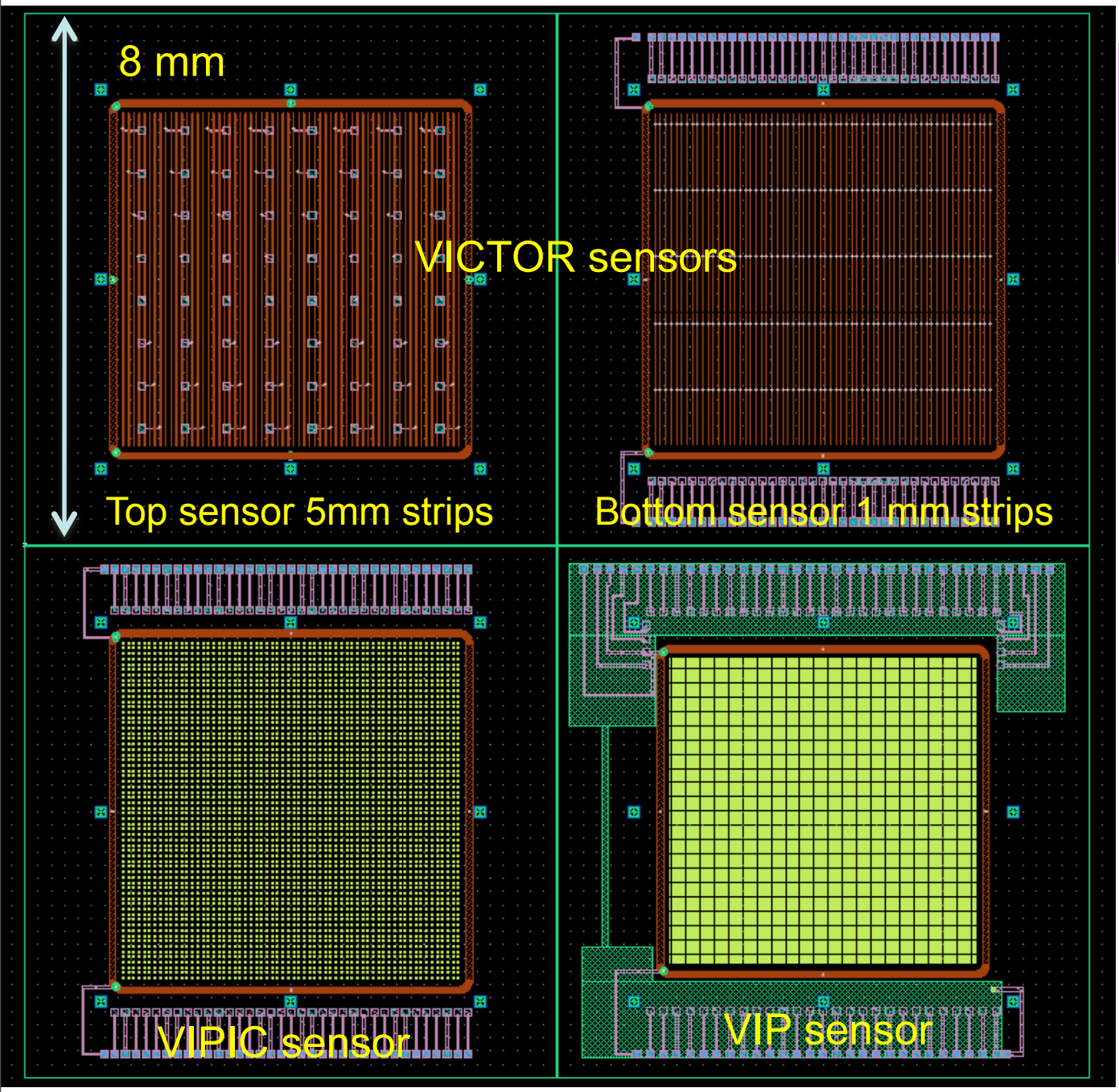


- Fermilab is organizing a multiproject run in the Tezzaron Process with a two-tier 3D wafer
- Process can include MAPS option
- Designs include:
  - Convert MIT LL VIP2a 3D design to the Tezzaron/Chartered process (VIP2b) - Fermilab ILC
  - Convert 2D MAPS device design for ILC to 3D design where PMOS devices are placed on the tier without sensing diodes – Italy ILC
  - CMOS pixels with one tier used as a sensitive volume and the second containing electronics. - France
  - Convert the current 0.25 um ATLAS pixel electronics to a 3D structure with separate analog and digital tiers in the Chartered 0.13 um process. – France sLHC
  - X-ray imaging/timing chip - Fermilab/BNL
  - 3D chip with structures to test feasibility of a 3D integrated stacked trigger layer. - Fermilab sLHC
- Now in Fab

Tezzaron MPW frame – each circuit contains right and left tiers after bonding

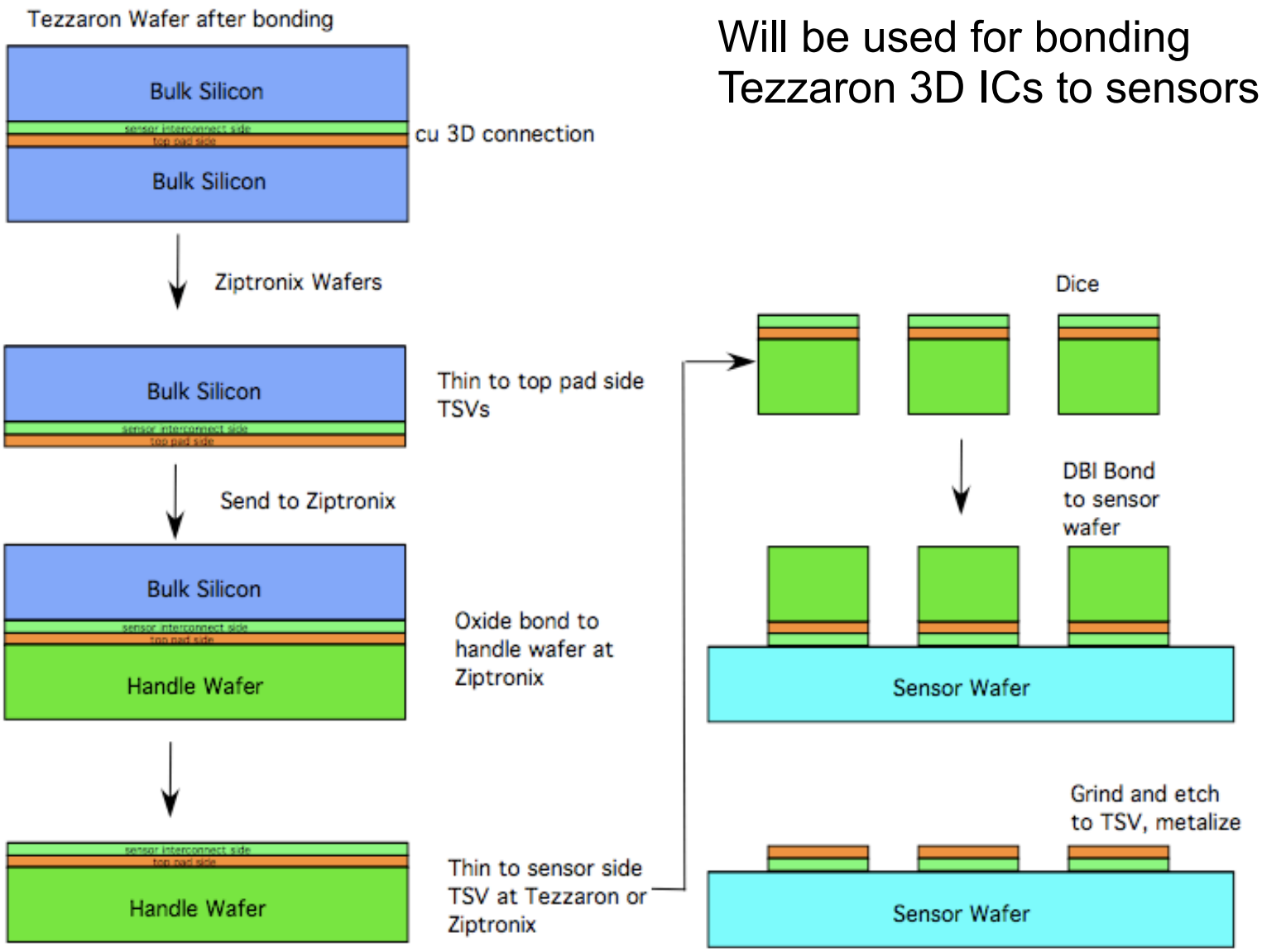
- VIP2b – Two –tier implementation of ILC VIP chip
- VIPIC - Vertically Integrated Photon Imaging Chip time stamping chip for x-ray imaging
- VICTR – 3D chip for sLHC CMS trigger





Mating Sensors (BNL)

3D Bonding/Tiling Process



Will be used for bonding Tezzaron 3D ICs to sensors

Application to x-ray imaging VIPIC

X-ray detection (8 keV) for X ray Pulse Correlated Spectroscopy with Si pixel detector

Intended to read out all hits in ~10μs window to provide time slicing for speckle analysis

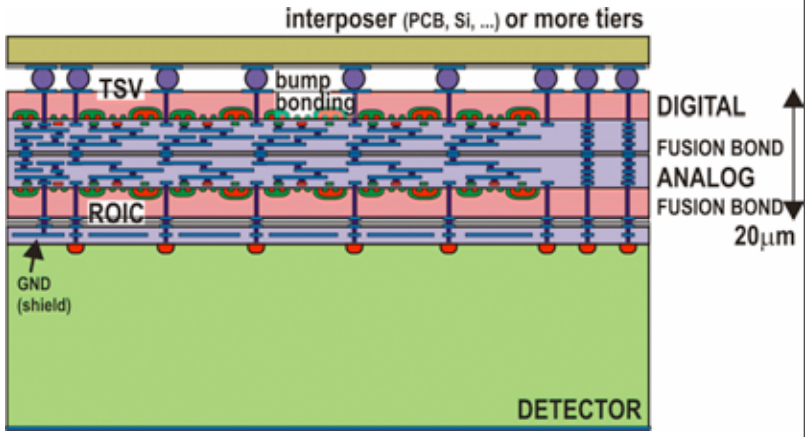
- 64×64 pixels, pixel area: 80×80 μm^2
- Separate analog and digital tiers
- trim DAC/pixel for offset corrections
- power consumption 25 μW/analog pixel
- CSA: noise ENC < 150 e-, τp < 250 ns, gain 115 mV / 8 keV Cfeed=8fF
- readout modes:
  - sparsified, binary readout (sparsified time slicing mode),
  - imaging binary readout mode (5 bit signal depth)
- dead-timeless and trigger-less operation in both readout modes
- two 5 bit counters per pixel for recording multiple hits per time slice (useable in the imaging mode)
- frame readout at 100 MHz serial readout clock
  - 160 ns / hit pixel in sparsified time slicing mode (up to 60 hit pixels / 10 μs)
  - 50×10^3 frame/s in imaging mode (5 bit counting)

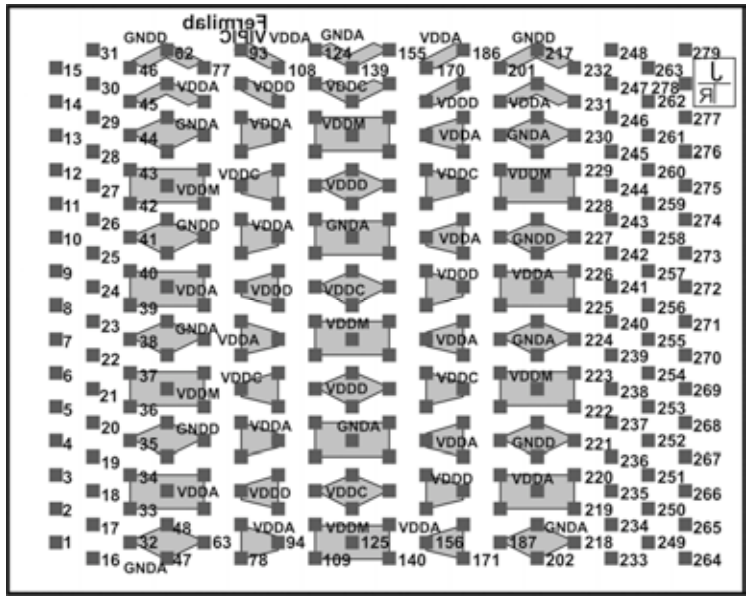
Integrated Focal Plane Arrays

These 3D technologies provide the ability to fabricate large area 4-side buttable arrays

- DBI can bond chips with 10 micron spacing
- Topside thinning provides access to interconnects over the full chip area
  - No dead area on edges for interconnects
  - Low impedance connection to ground and power planes
  - Good shielding
- Separation of analog and digital circuit layers

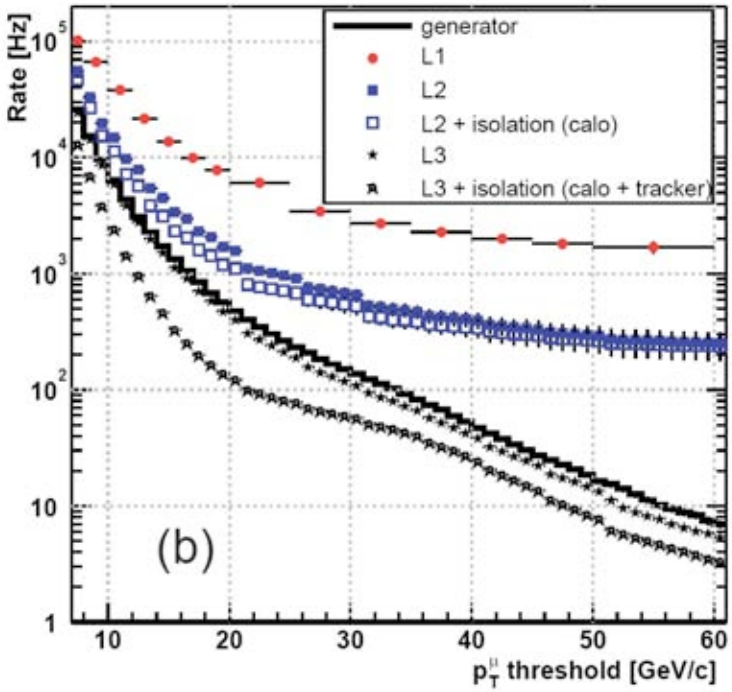
We hope to demonstrate this with the VIPIC and VIP chips in the Tezzaron/Ziptronix run



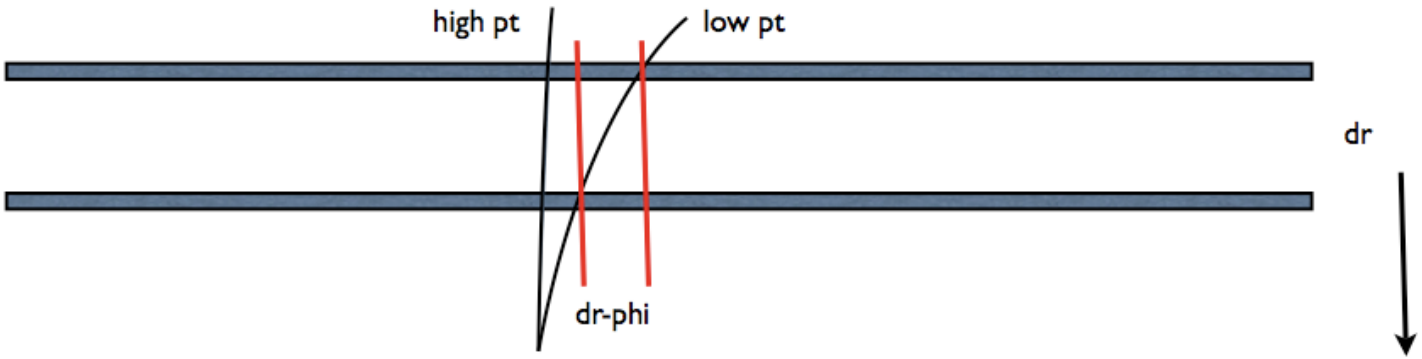


Application of 3D to a Track Trigger

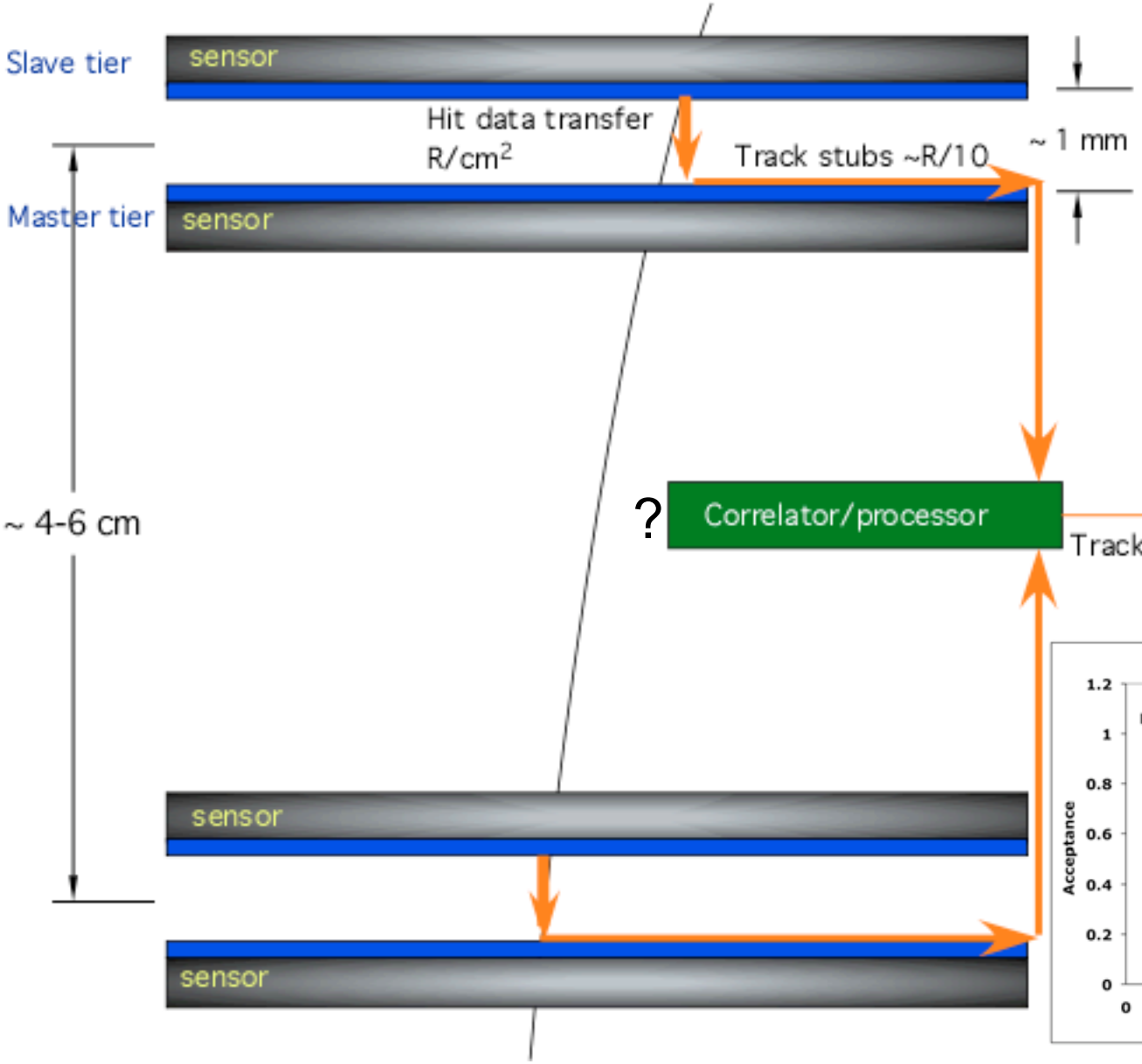
- The standard lepton and jet triggers at CMS in sLHC will saturate - track information will be needed to achieve acceptable rates.
- The power and bandwidth needed to collect all of the information generated by a pixelated tracker in a central trigger "box" makes local momentum-based hit filtering crucial
  - 4-8x10^7 hits/cm2 sec at r~34 cm



- What we would really like to do is locally (=low data transfer power) correlate hit information to transfer information relevant to moderate pt tracks for fitting.
  This is exactly the capability that vertical integration provides

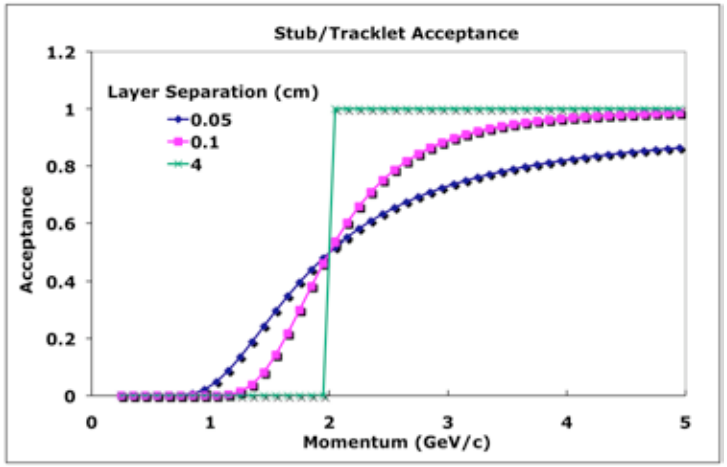


Double Stack Concept



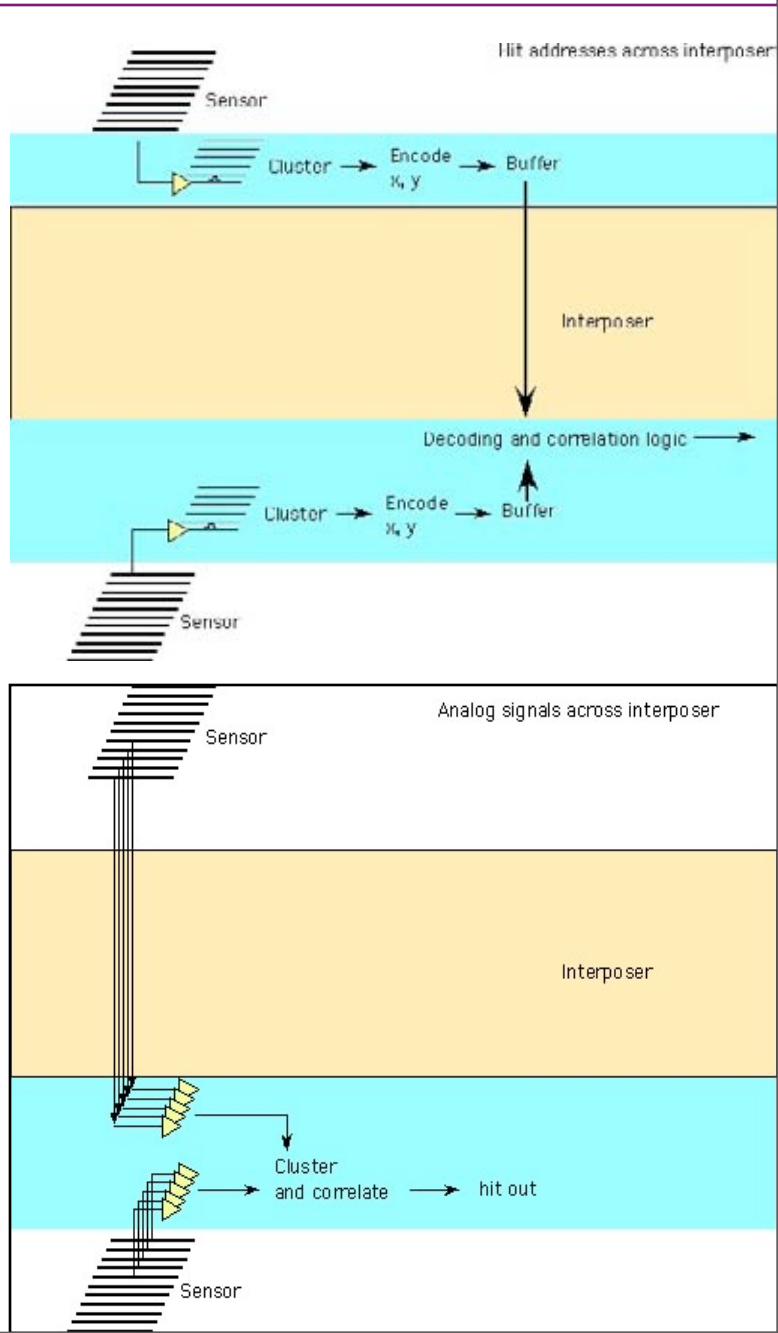
Data flow:
- Hit information flows from top to bottom tier
- Bottom (master) tier looks for local correlations, filters clusters, and sends data off-module
- Stubs are sent off the rod to a processor which forms local tracks (tracklets) and tracks.

Spreadsheet estimate

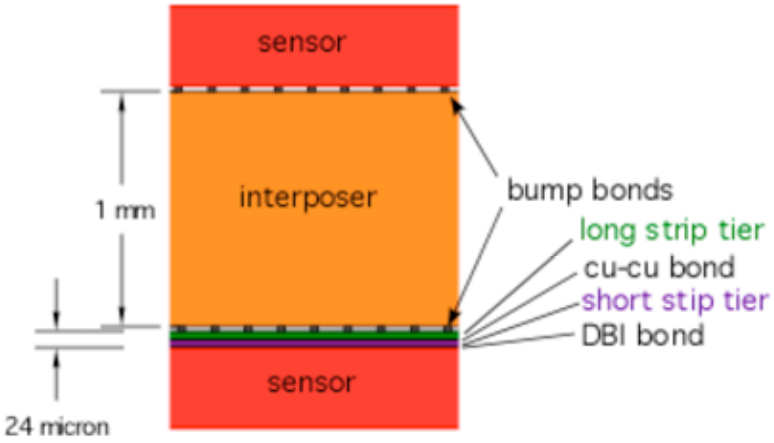


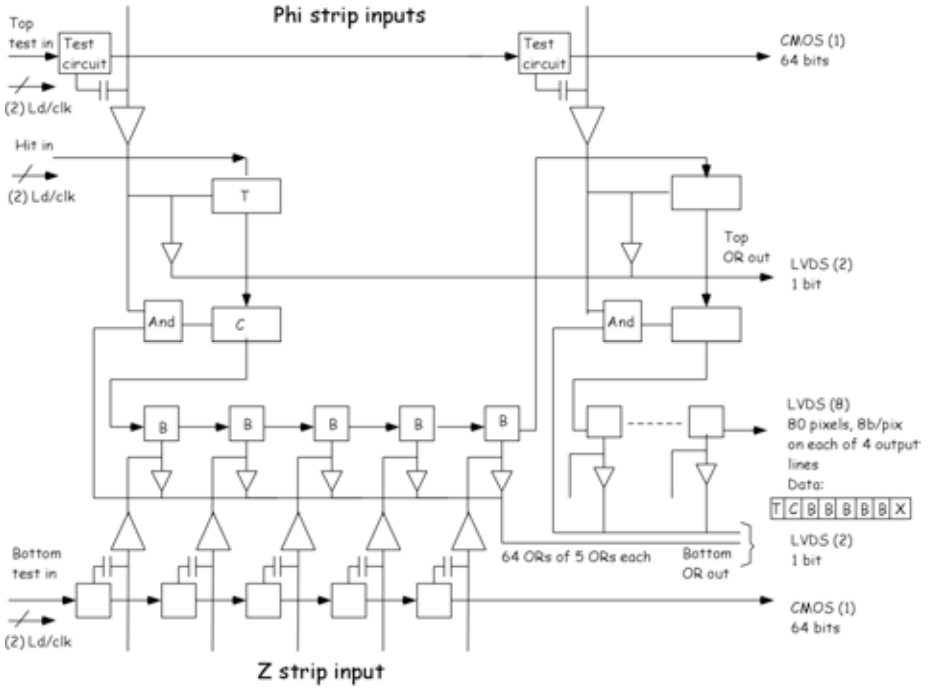
Module Architecture

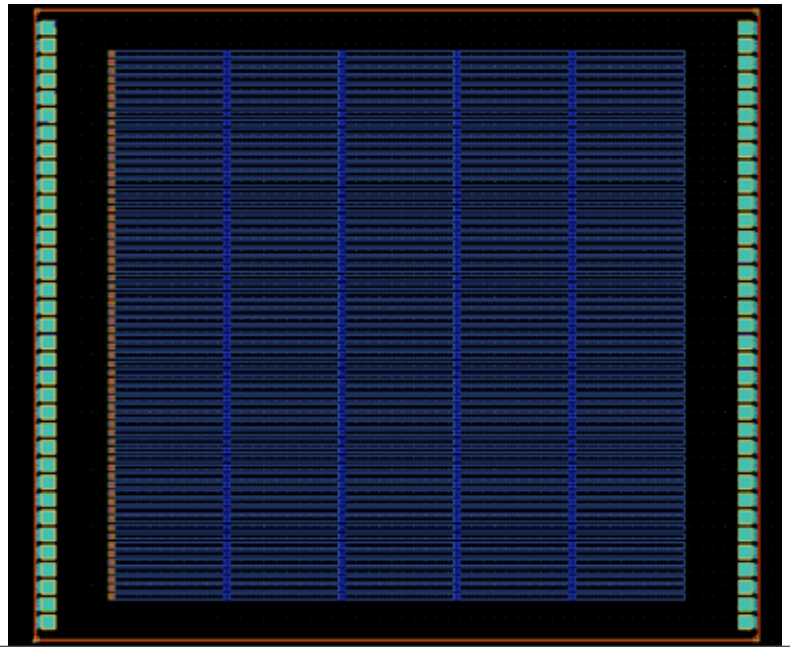
- Strawman - Local doublet, sensors separated by 1mm, with initial cut at ~2 GeV
- Two sensors separated by a mechanical spacer (like a circuit board)
  - Spacer (called interposer) carries utilities and inter-chip communication
- Sensors have chips directly bonded (DBI) to them
  - Hit information transferred vertically at high density utilizing through-silicon vias available in 3D technologies
- Chips have both readout and trigger functions
- Interposer character depends on optimization of the design
  - Clustered and encoded data sent ~32 vias/ cm2 (low via density, high rate)
  - Analog data sent from sensor - 1 interposer via/channel (high density, low rate, low power)

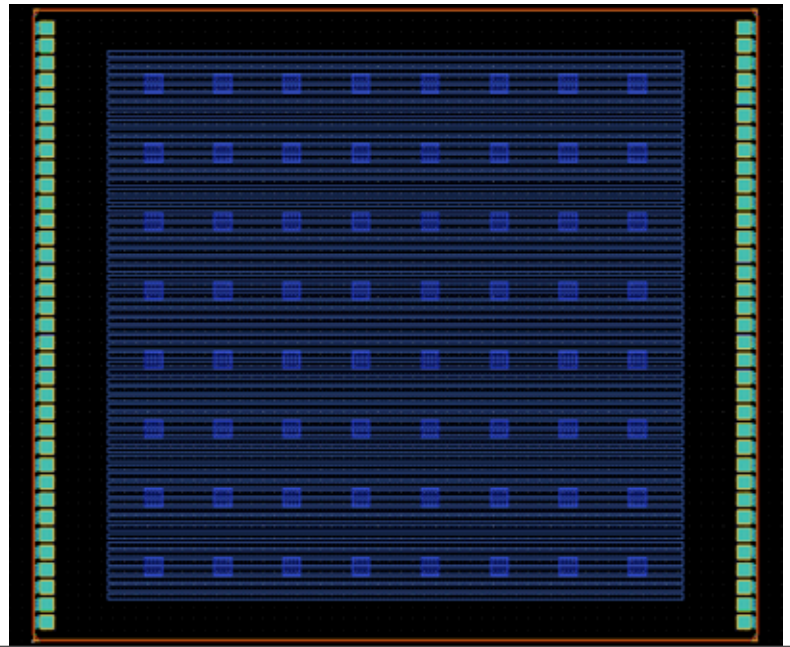


VICTR- Vertically Integrated CMS TRigger Chip

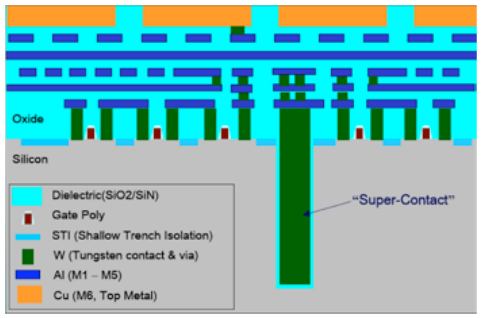




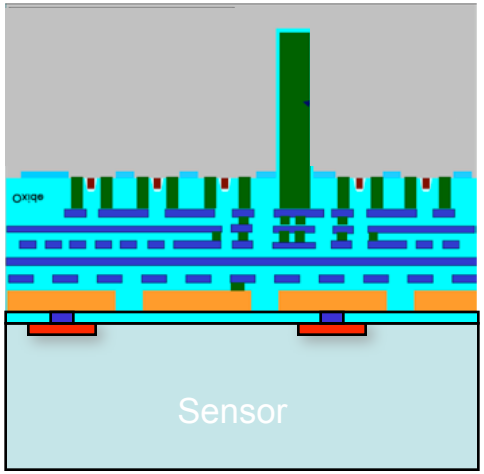




Doublet Layer Construction

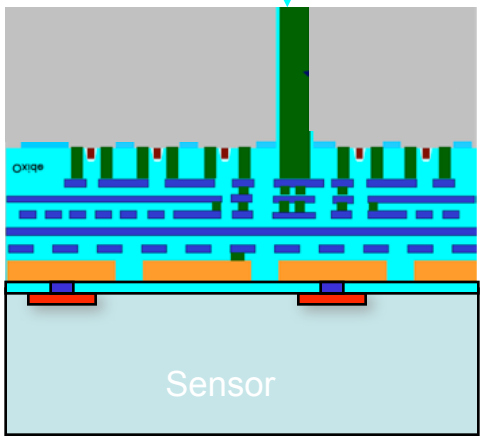


Readout IC wafer with TSV from foundry

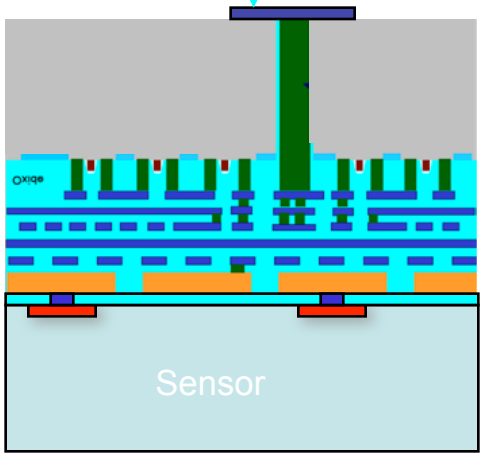


DBI bond

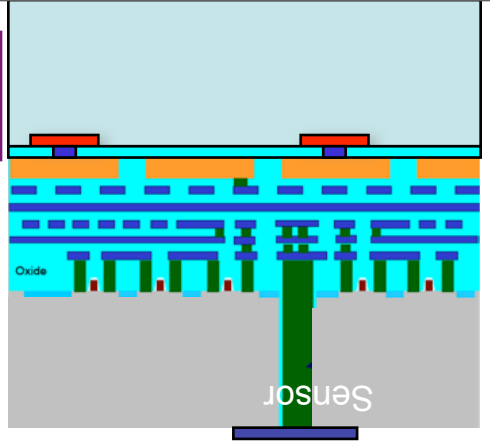
Oxide bond diced ROIC to sensor Wafer.

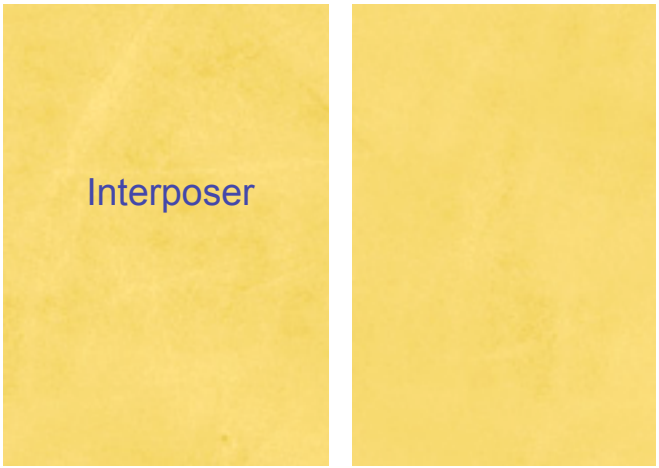


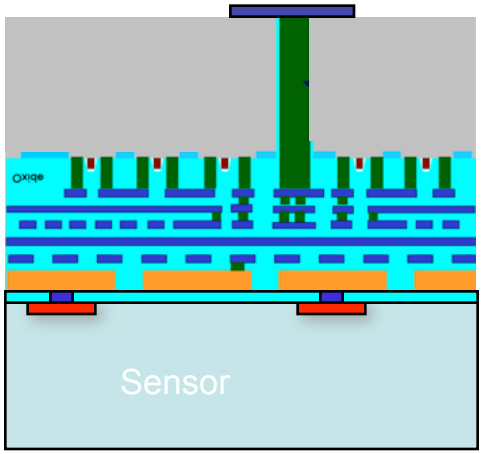
Thin to expose TSV



Contact lithography provides
Access to topside pads for vertical data path

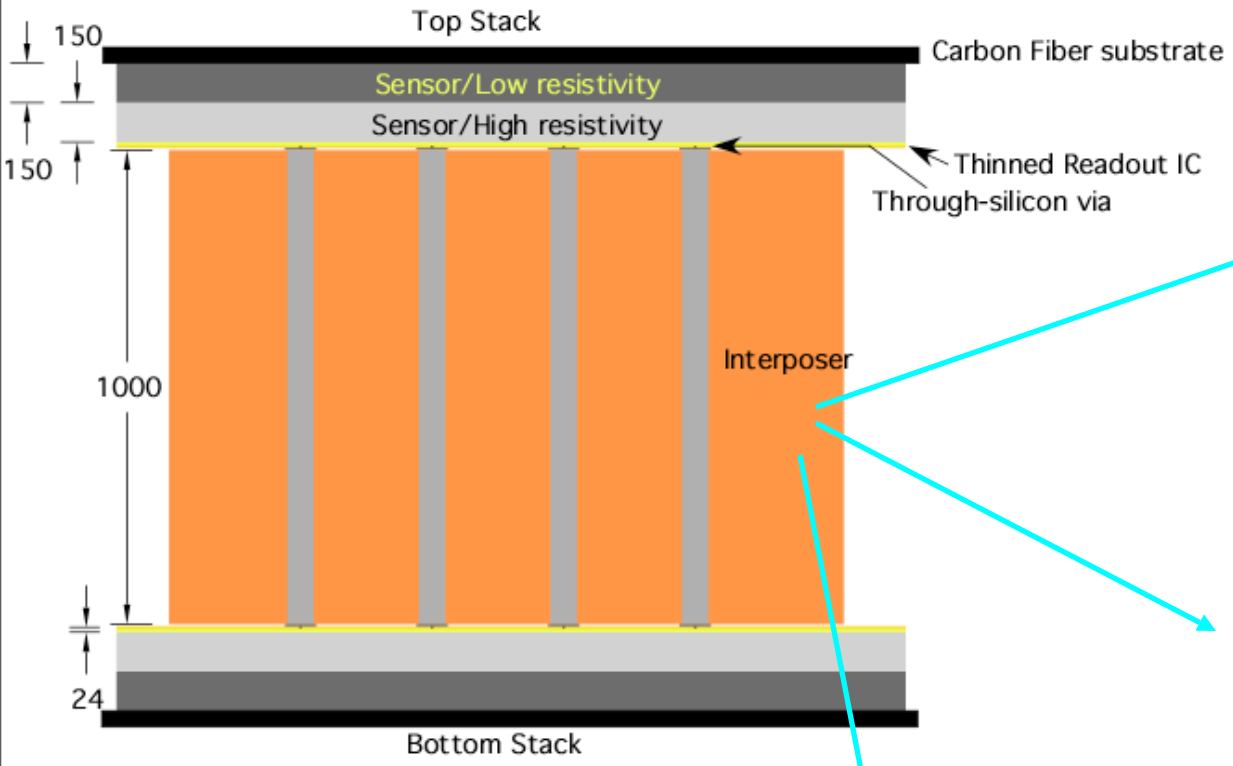




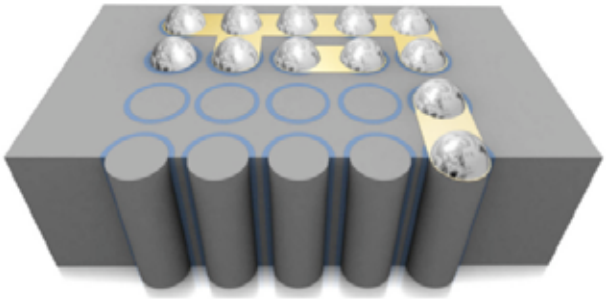


Bump Bond module

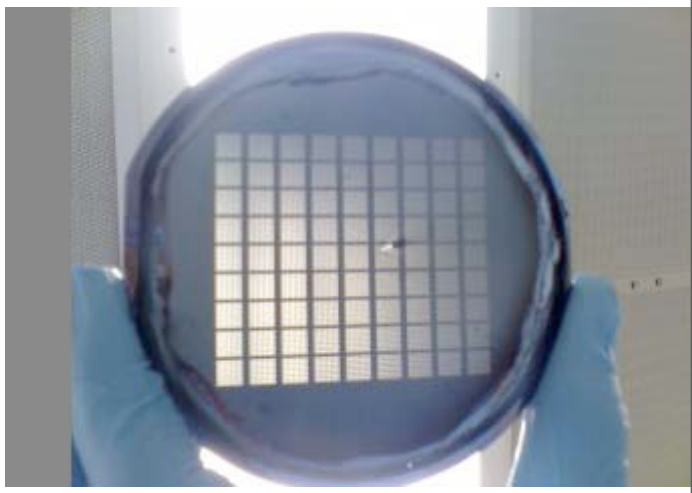
Test, assemble module with interposer



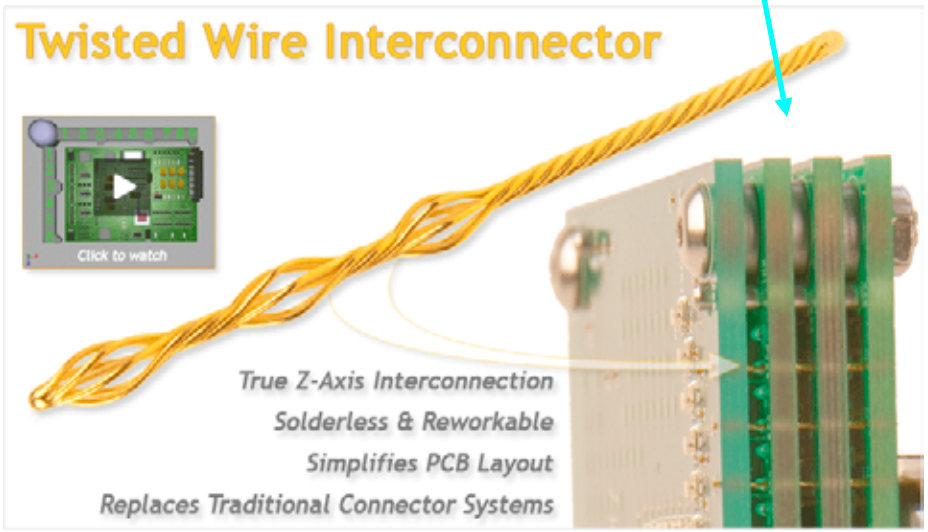
units are microns, horizontal scale arbitrary



All-silicon vias (Silex)

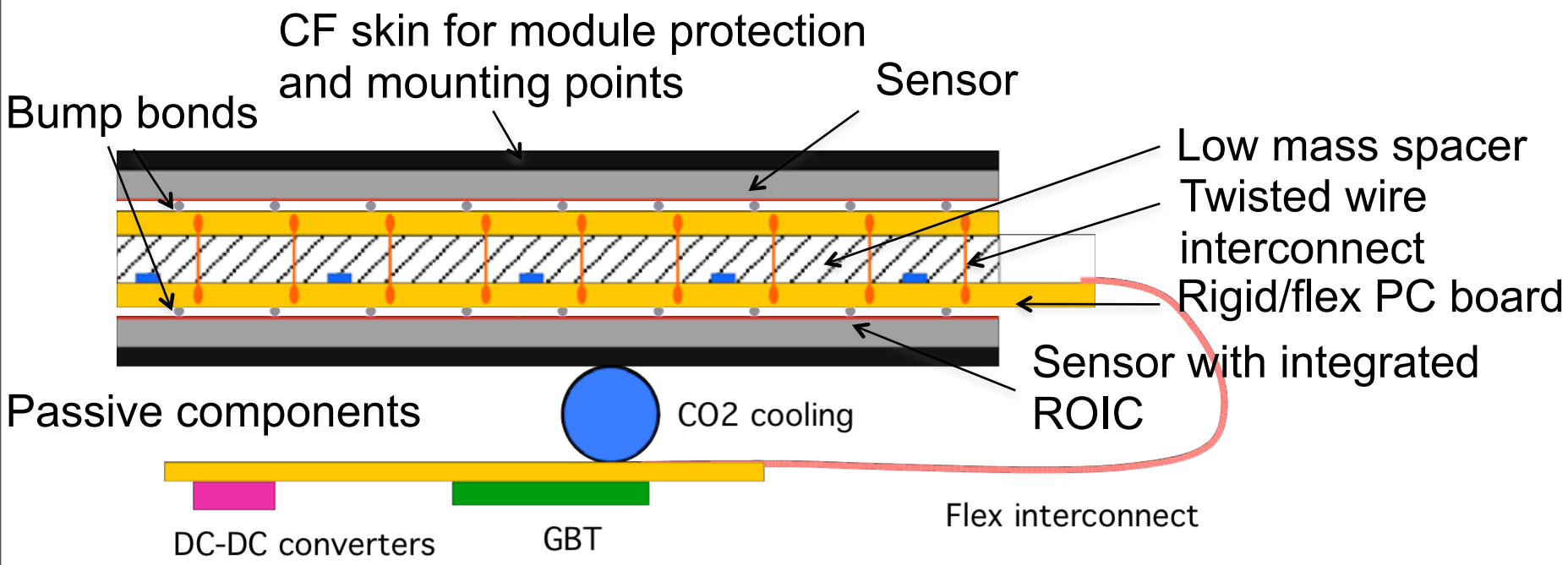


Test Interposer (Cornell)



Options for interposer depend on inter-layer connection density, mechanical, cooling considerations - important optimization problem

Vertically Interconnected Module conceptual design



Physically robust module

Power hungry parts near cooling

Provides electrical interconnect paths which should be conventional

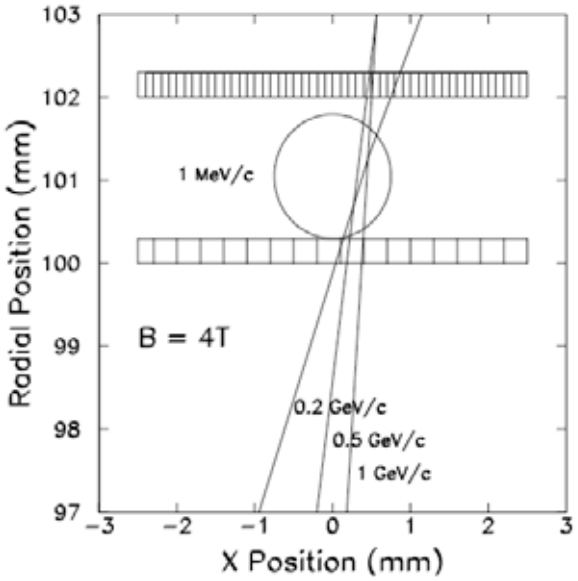
- Needs 2 layers of bump bonding
- Relies on vertical interconnection of sensors and Ics

A rad-hard SOI or MAPS technology would also work

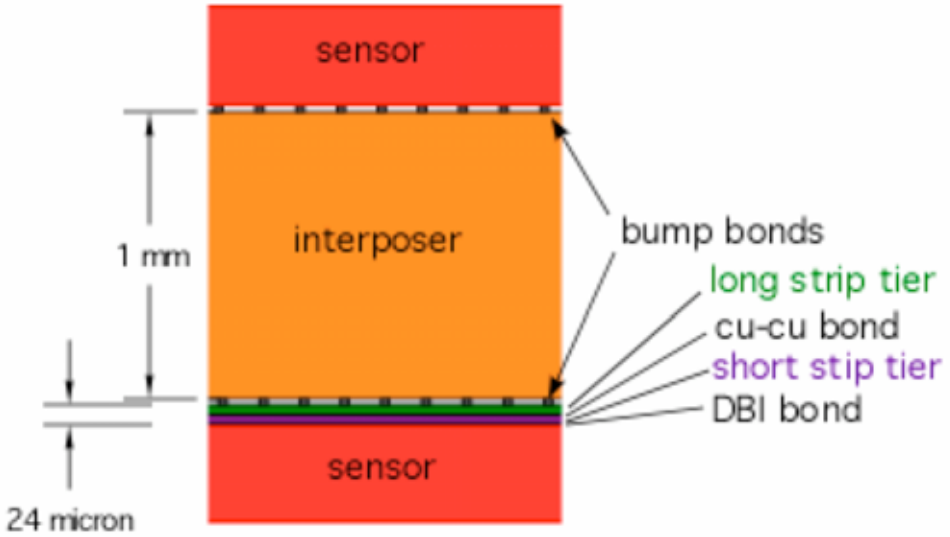
Back to Leptons

Muon Collider VTX

- 20th Century studies assumed 300 μm square pixels
- ILC studies now assume ~ 20 μm square pixels x 225 less occupancy/ pixel
- S. Geer suggested a stacked layer design to reduce occupancy based on inter-layer correlations for the muon collider in 1998
- This technology looks very much like what we are developing for the CMS upgrade



1999 μCol Track correlation module



2009 Track trigger module for CMS Phase II Based on 3D electronics

The Vertex Detector Commandments

1. Thou shalt minimize mass
   – thinning and bonding
- Thou shalt have high bandwidth
  – vertical interconnection
- Thou shalt be radiation hard
  – thin detectors, deep submicron
- Thou shalt not dissipate power – low node capacitance, short interconnects, limit digital activity
- Thou shalt have complex functionality – multiple layers with optimized technology
- Thou shalt maximize resolution– fine interconnect pitch, multiple readout layers
- Thou shalt minimize dead regions – 4 side buttable Ics
- Thou not covet thy neighbors signals – isolated layers, minimize crosstalk

Conclusions

- Advances in IC technology are providing exciting opportunities for low mass, high resolution vertex detectors
  - A chance for HEP to return to the forefront
- R&D inspired by the ILC but there are compelling applications to low power, low mass, high resolution silicon arrays
  - Size of the pixel can certainly be reduced (no bump bonding)
    - DBI allows very fine pitch and excellent mechanical strength
  - Think about how multiple layers of electronics can effect how a pixel detector is designed (process fields of pixels…)
  - Optimization for low power and mass
- Other applications:
  - Synchrotron radiation detectors
  - Electron microscopy
  - K+-> π+νν beam telescope
  - Muon collider
  - …

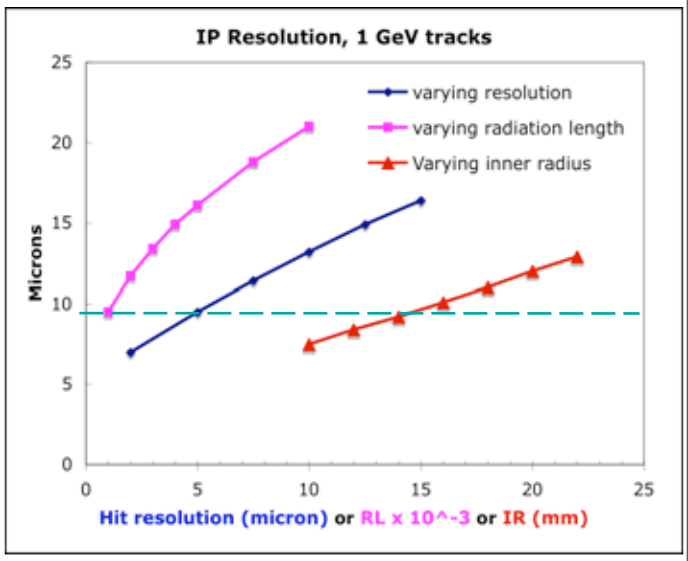
ILC Vertex Detector

Basic goals are extrapolated from the SLD CCD vertex detector:

- Excellent spacepoint precision (< 5 microns)
- Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
- Transparency (~0.1% X_0 per layer)
  - Power constraint based on minimal mass
- Integration over <150 bunch crossings (45 msec)
- Electromagnetic Interference (EMI) immunity
- Moderately radiation hard (<1 MRad)
- Stand-alone pattern recognition (SiD)

Power and mass are the most significant challenges

CLIC adds time resolution to above

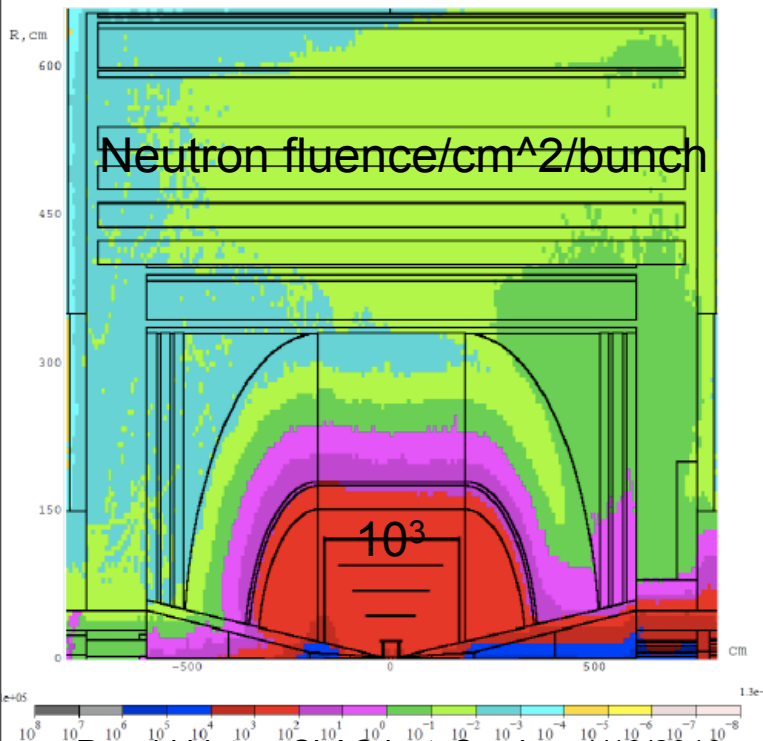


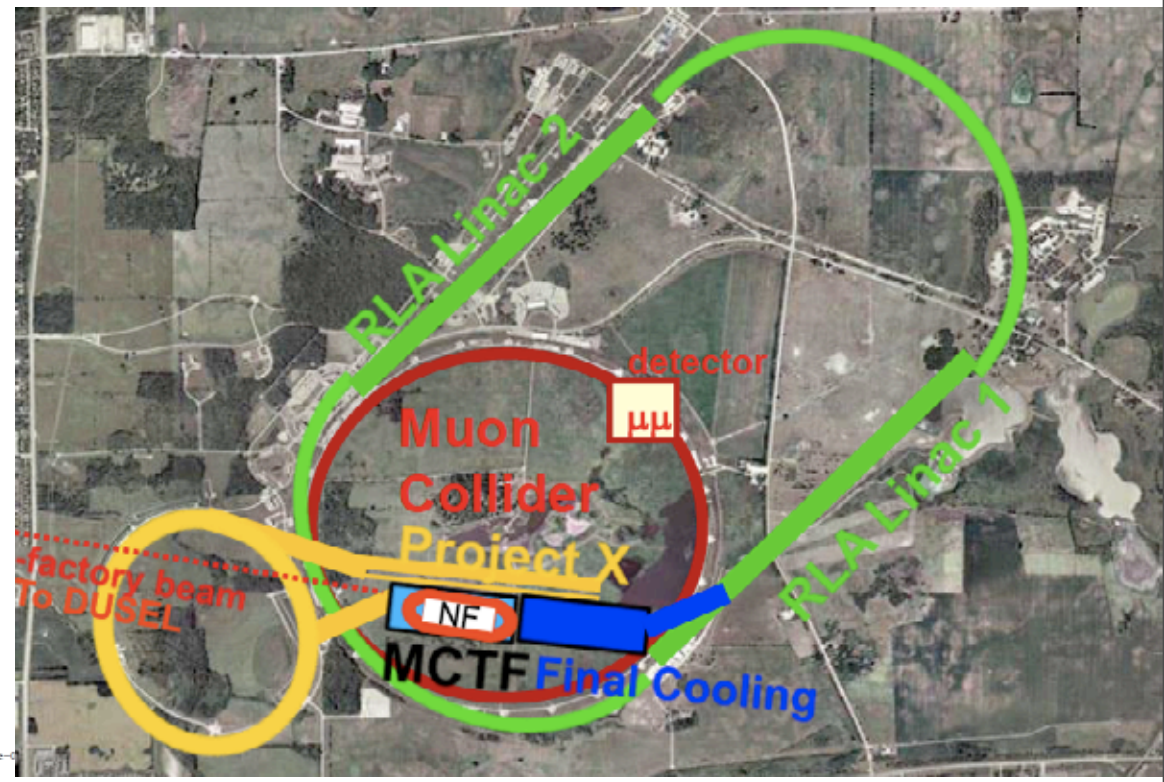
Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resolution
- 1.4 cm inner radius

Varying each parameter

Muon Collider

- Recent workshop at Fermilab to begin studies of muon collider physics
  - 1-3 TeV muon collider on site
  - Many accelerator issues
  - Site radiation issues – a shallow site exceeds site boundary radiation limits due to *neutrino* interactions
  - Detector backgrounds





Muon Collider and LHC

- 1 Mgy = 100 Mrad
- Need to scale all particle fluxes to NIEL damage, then compare to LHC
- μColl similar to sLHC