Strip Upgrades and Trigger

July 17, 2009
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LBNL
For the ATLAS Strip Upgrade Collaborations
Introduction

• In current ATLAS, outside pixels have long (12 cm) strip layers (SCT) and straw tubes (TRT).
• This system is expected to operate until the Phase 2 period.
• For Phase 2 (install in 2019) the SCT+TRT should be replaced with an all-silicon system
  – Increased granularity (up to 400 evts/crossing)
  – Increased radiation resistance
  – Control mass
  – Possible trigger capability
• The strip upgrade is an active R&D and prototyping project
  – Considerable development in across ATLAS, extending to 2012
  – Many workshops, regular working group meetings
  – R&D management structure in place
  – Many baseline electrical and mechanical aspects have been selected
  – LOI organized, submit in 5/2010, TP in 2012
Now and Then

Present ATLAS SCT 61 m²
~ 4K modules, precision mounted with~ 5 μm internal build required
• Modules rigid and self supporting
• Heat flows across the plane
• Individual power, DAQ to each module
• Significant fault tolerance
Phase 2: ~20K modules + services!
Current Phase 2 ID Layout

- 5 double sided barrel layers
  - Inner layers: 3 of 2.5 cm = short strips
  - Outer layers 2 of 10 cm = long strips
- 5 double sided disk layers
- Basic substructure is a “stave” or “petal” being a highly integrated electrical/mechanical/thermal element holding many “modules”
- A number of new technical challenges…due to radiation, scale, performance
Barrel Staves

~ 1.2 meter

Bus cable
Hybrids
Carbon honeycomb or foam
Coolant tube structure
Readout IC’s
Carbon fiber facing

SLAC LHC Wkshp.
Forward Petals

Valencia

• Challenge in forward region is to limit the multiplicity of sensor and module designs and to efficiently use TTC and power distribution resources
Staves and Petals

- Staves front load much of the tracker assembly and integration
  - Embed in a simple insertion scheme
- Staves offer an efficient cooling scheme due to embedded coolant
- Staves are a minimal mass solution
- Staves provide a natural structure for local triggering doublets
- While not exclusive to the stave, propose a highly multiplexed TTC and efficient power distribution scheme
  - Multi-drop clocks, addressing, and commands
  - Alternative powering schemes including serial and DC-DC conversion
  - A way to dramatically reduce the electrical services
Enabling Technologies

- All of these are areas of active development in the collaboration
- Sensors: enhanced radiation resistance, p bulk
- Front End ASICs designed to SLHC specifications
  - Low noise to complement CCE loss due to radiation
  - Fast data readout
  - Integrated power regulation
- Hybrids: low mass, high density flex laminates
- Modules: hybrids glued to sensor, proximity
- Power and signal distribution:
  - Embedded bus/shields,
  - Multi-drop
  - Alternative powering
- Mechanical support and cooling: composites, large ΔT
- Assembly and inspection methods: precision fixturing, robots
- DAQ: high speed data I/O for multi-modules in parallel
Upgrade R&D Organization

Proposed Organogram for ID strips in Lol/Stave09 period

ID

- Strips Abe Seiden
  Dep: Phil Allport

  - Sensors: Nobu Unno
  - ASICS: Francis Anghinolfi

  Kids

  - Pixels

  - Modules
    - Ulj Parzefall (F)
      Dep: Tony Affolder (B)
    - Barrel Staves
      D. Lynn
      Dep. ?
    - Endcap Staves
      Carlos Lacasta
      Dep. ?

  - Stave09/Electrical
    Carl Haber
    Dep: Dave Robinson

    - Electrical Interfaces
      D. Ferrere?
      Dep. ?

Across ID

- Electronics
  Philippe Farhiouat

- Thermal Management
  Georg Viehauser

- Powering
  Marc Weber

- Optolinks
  Clgdem Iseever/KK Gan

- Engineering
  Andrea Catinacchio

- Services PP2 Out
  Sigl Wenig

- Layout
  Leo Rossii?

- Simulation
  Jeff Tseung

- Radiation and shielding
  Ian Dawson

- DCS
  Didier Ferrere

Thermo-mechanical design
Interface to ID-services
Insertion-mechanics
Prototyping

Thermo-mechanical design
Interface to ID-services
Insertion-mechanics
Prototyping

Set up central Facility
Bus Cable
Test-DAQ
Powering
HV
Cooling
DCS

DAQ
DCS
Off-detector Interface to electrical and optical services

19 June 2009
Large Area P-type Sensors

- Because of advantages after heavy irradiation from collecting electrons on n+ implants, the detectors at the LHC (ATLAS and CMS Pixels and LHCb Vertex Locator) have all adopted the n+ in n- configuration for doses of $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$
- Requires 2-sided lithography
- Starting with a p-type substrate offers the advantages of single-sided processing while keeping n+-side read-out
- Processing Costs (~50% cheaper).
- Greater potential choice of suppliers.
- High fields always on the same side.
- Easy of handling during testing.
- No delicate back-side implanted structures.
- Series of full size and miniature “ATLAS07” prototypes have been made with various isolation structures.
ATLAS07 Mini’s: Proton Irradiations

- Irradiations performed to 2.3, 6, \(1.3 \times 10^{14}\) \(n\) \(\text{cm}^{-2}\) with 70 MeV Proton

ATLAS07 perform as expected
- At 500 V, \(2.3 \times 10^{14}\) \(n_{\text{eq}}\) \(\text{cm}^{-2}\): 17-21 ke-
- At 500 V, \(6 \times 10^{14}\) \(n_{\text{eq}}\) \(\text{cm}^{-2}\): 16-19 ke-
- At 500 V, \(1.3 \times 10^{15}\) \(n_{\text{eq}}\) \(\text{cm}^{-2}\): 11-14 ke-

Reasonably good agreement between different sites, systems, analyses and measurement techniques

Measured noise of ABCN25 on module with Hamamatsu sensor and 20 chip hybrid of 650 e-
ATLAS Binary Strip Readout

- As with the present SCT, the upgrade will use a binary readout scheme. (Atlas Binary Chip)
- Register hits only
- SCT used DMILL BiCMOS technology, for upgrade move to DSM CMOS
- New development ABC-Next
- Clock FE pipeline at 40 MHz
- Clock data out of chips at 80 MHz but multiplex two data streams to 160 MHz.
- V1 in-hand and operating

![Diagram of occupancy, Vt_50, and V threshold vs. Charge injected]
# ABC-Next Front End Development

| Front-End | Optimised for short strip but power tuning capability for long strips | 27mA/chip (tuneable) ✓
|           |                                                                   | 750enc (2.5cm strips) Final S/N > 10 ✓ |
| Back-End  | Main change in DCL block to 80MHz                                  | 92-96mA/chip at 2.5V nominal |
| Powering  | 2 integrated shunt regulators schemes                             | Current limiting option to impose uniformity |
| Floor Plan | Width to allow direct bonding to sensors                           | |
| Data Buffering | Pipeline and derandomizer implemented                           | |
| Submission | June 2008 (IBM 0.25μm)                                            | Delivered end October 08 |

Francis Anghinolfi
20 Chip Hybrid for Barrel Modules

SCT DAQ Read-out adapted for ABCnext by Cambridge, RAL, Liverpool

80MHz data rate (10 x ABCn)

Gain: 100mV/fC
Input Noise: ≤400 enc
Threshold variation before trimming: 5.5mV
after trimming: 1mV

A. Greenall
A. Affolder
Liverpool

- Gain and Input noise show very little change.
- Data/token passing works at 80MHz.
- Tested using Front-end regulator enabled.
Alternative Powering Schemes

- **DC-DC conversion** – High voltage in, step down to 2V and 4A, most likely would use a multi-step approach
  - Under study – buck conversion with COTS and custom parts
  - Charge pump ASICs
  - But still needs detailed noise and interference studies
- **Serial Power** – recycle the current
  - Detailed proof-of-principle using SCT generation components
  - Regulators included in ABC-Next
  - Monitoring, control, and bypass circuits are under development and will be included in upcoming prototype staves

Yale/RAL/BNL/CERN
Stave Hybrid

- 20 chip hybrid for stave (Liverpool)
- Includes TTC interface for multidrop and AC coupling, addressing for multi-modules
- Buffer Control Chip (BCC) designed at SLAC, now in hand and functional
- Powering options board to allow tests of DC-DC and serial powering, bypass and monitoring on a stave (RAL, BNL, Yale)
Bus Cable Layout

- Al shield
- Data readout 1/hybrid
- Clock & Command lines
- Port Card (passive SMC)
- Serial current return
- HV distribution
- Serial current link
Early Test of Stave and Modules

- Test vehicle for electrical performance studies using SCT chips and COTS parts
  - Noise
  - Cross talk
  - Grounding, bias, and shielding
  - Signal propagation
- Module is serially powered, AC coupled data and control
- Good noise performance observed on stave, studies continue
- Tested with a range of substrates, thicknesses

![INPUT NOISE vs STRIP LENGTH](image)

<table>
<thead>
<tr>
<th>LENGTH (CM)</th>
<th>NOISE (ELECTRONS)</th>
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<tr>
<td>0</td>
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</tr>
<tr>
<td>5</td>
<td>500</td>
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<tr>
<td>10</td>
<td>1000</td>
</tr>
<tr>
<td>15</td>
<td>1500</td>
</tr>
</tbody>
</table>

CC 200 um
BeO 200 um
Epolite FH 5153 50 – 75 um or alternative
First SLHC Short-strip Module Demonstrator

- Both fully loaded 20 chip hybrids
- ABC-Next chips
- ATLAS07 p-type sensor
- One hybrid glued directly to silicon, one bridged over Al
- Good noise performance in either case, 650 e @ 2.5 cm
Glued Sensor Irradiation Studies

Irradiated to $1.5 \times 10^{15}$ p cm$^{-2}$ at CERN ($9.3 \times 10^{14}$ n$_{eq}$ cm$^{-2}$)
No measurable effect of glue relative to similar irradiations

Using fit of clustered charge, efficiency at 500 V near 100% at threshold of 1 fC for 1×1 cm$^2$. Would expect 0.75 fC needed for 2.5 cm strips.
Stave-DAQ: Multi-module System

SLAC board development

HSIO BOARD

s/w: UK, LBL
Prototype Stave Core Construction

BNL, Yale
LBNL
RAL
Oxford
Summary of Baseline Effort

- Well organized and active collaboration addressing a broad range of technical issues
- Significant early progress on all aspects – sensors, FEE, modules….
- Many details but no show-stoppers at present
- Major focus of next year will be a full scale ATLAS specific short strip stave “Stave-09”
- Build up technical base also at CERN over next year
- LOI preparations
- Uncertainties
  - Continued schedule shift
  - Need for track trigger…
Need for a L1 Trigger

- ATLAS (and CMS) do not presently use Inner Detector in the L1 trigger
- Not considered technically feasible in past
- L1 track trigger creates new primitives ($p_T$ tagged track vectors) which combined with $\mu$, $e$, $E_T$, etc., offer new physics tools
- A high luminosity this could be crucial
  - Flattening of muon trigger above 20 GeV
  - Addition effect of cavern backgrounds could introduce excessive fake rates in the muon trigger, false triggers are flat in $p_T$
- Enabling technologies
  - FE chips, high density interconnects, data transmission, trigger processors
L1 Trigger Effect

- All four recent ATLAS workshops had significant input on triggers
- Muons:
  - The rate flattens off above ~20 GeV, similar to CMS
  - Mainly resolution effect, 20 GeV ~ ∞ but also low BL² regions and other effects
  - Can look into muon solutions to improve this – certainly the LVL2 and EF improve significantly so there is scope

![Single muon trigger](image)
Approaches

• ROI readout of ID for high-rate L0.5Calo/Muon trigger
  – E.g. 10 % at 400 kHz --> limited impact on average ID bandwidth
• Storing tracker data longer in FE at L1 and dropping if fast-clear given
  – Allows more time for L1Calo and L1 Muon combinations
• Coincidences for parallel strips a few mm apart
  – Silicon sensor pairs with local hit correlations,
  – A development of local intelligence within the tracker, data driven
  – Natural application of the stave and petal concepts
• ~17 mm gaseous detector (micromegas) at outer layers
  – Measure track stub
Sensor Pairs

For reasonable pitches, sensor separations, and momenta find ~7 bins
Local module output could be 3 bits : 7 bins + 1 sign
Technical Concept

Sensor ~10 x 10 cm
Fine pitch interconnect
Digital chip on hybrid
Bus cable
Analog chip on hybrid
Wrap around
digital chip
pre-amp disc
trigger
output
pipeline
n
n+1
Wrap around
Already similar to baseline stave…
Future Trigger Directions

• Track trigger working group convened by R. Brenner
• Ongoing simulation and performance studies underway
• Featured in dedicated sessions at Tracker Upgrade meetings
• ATLAS-CMS common discussions and efforts?
• Generic R&D on trigger concepts
• Hardware oriented workshop open to non-ATLAS as well
  – Jan 26-28, 2010 at Lawrence Berkeley National Lab