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SLC Control Program

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SLAC's Software Engineering Newsletter

July 22, 1993 | **All that Fits is News to Print** | Vol. 7, No. 4

History Buffer Correlations

July 7, 1993

Author: *Puzo, White* **Subsystem:** *SLC* **User Impact:** *Small*
Panel Changes: *Few* **Documents:** *No* **Help File:** *Yes*

History Buffer Correlation software is becoming smarter and smarter.

Up until now, you always had to enter a complete device name including primary, micro, unit, *etc.* even if you just wanted to change one component of a previously entered name. With this release of the software, if a device has already been entered, you can omit entering the components you wish to keep unchanged. So you may enter only the channel, or the unit number, or the secondary.

For example, if you select [ENTER DEVICE NAME] for variable A, you get the prompt: "ENTER PRIM [ ]:". You can type "KLYS,TL00,1,ADES". Now if you select [ENTER DEVICE NAME] for variable B, the prompt will be: "ENTER PRIM [KLYS]:" at which point you can ignore the primary and micro prompt and just enter "11,AJTN". The two variables will now be:

A = "KLYS TL00 1 ADES"

B = "KLYS TL00 11 AJTN"

When entering a channel number, it is no longer necessary to prefix it with '#'.

Also, the data filtering function has been removed from plots of A vs B under manual scaling. Previously, manual scaling in A vs B plots was performed by cutting the data points outside the specified ranges, and then plotting all the remaining points. Since the time stamps of B were aligned with those of A, these plots sometimes produced confusing results. The algorithm has been changed so that now no points are removed, but only those within the manual scaling ranges are plotted.

SLD CDC High Voltage and SLC Wirescans

June 29, 1993

Author: *Yasukawa, Chestnut* **Subsystem:** *Final Focus* **User Impact:** *Small*
Panel Changes: *None* **Documents:** *No* **Help File:** *None*

There is now a system in place by which the SLD CDC High Voltage can be at a safe level whenever ETA wirescans are performed which could spray particles into the inner chambers and cause a high voltage trip. The communications involve three signals which are sent via IDIM/IDOM pairs. One signal from SLD indicates that SLD will NOT honor requests to lower the HV, negotiations are necessary. The next signal is from SLC to SLD indicating a request for SLD to lower the voltage, and the third signal is the acknowledgement from SLD that the voltage has been lowered.

Code in the SCP checks the old SAFE or TUNE states, then if necessary, looks for permission to request a lower voltage. It then requests a lower voltage and loops for three minutes (the timeout countdown appears as a button shadow) checking every five seconds for SLD readiness.

This code is meant to be used for the incoming beam of the eta wires (FF11 3345 and 3845 and FF01 3345 and 3845) when SLD readings can be disturbed. The communication is triggered when the HSTA bit of x'0100' is set. When outgoing beams are scanned, the x'0100' can be cleared and no requests are made to SLD.

Three type of events lead to the SLD communication when the HSTA bit is set:

1. single wire scans,
2. using the eta wire package, and
3. doing correlation plots with PHYS variables from the eta wire package.

Since there may be some problems when lowering and raising SLD voltages, SLD has requested to be called when an eta wire is going to be scanned in case any software problems occur. Their contact point is Ron Cassell.

CUD Enhancements and Fixes

June 24, 1993

Author: *Daniel Van Olst* **Subsystem:** *CUD* **User Impact:** *Very Small*
Panel Changes: *Very Few* **Documents:** *No* **Help File:** *Yes*

Several fixes and enhancements have been recently made to the CUD Facility.

- Previously, if a new updating interval for a CUD display was entered from the SCP, it would not go into effect until the CUD process was restarted with WARMSLC. This problem has been corrected so that new intervals are implemented immediately.
- There has been some confusion regarding the difference between the CUD BPM displays and the CUD BPMALL display.

The CUD BPM displays may either be set to DIFFTMT or ABSOLUTE; this indicates how the data is displayed.

The CUD BPM displays may also be set to CYCLE or NOCYCLE; this has no effect on the CUD BPM displays themselves, but rather indicates whether the CUD BPM display is displayed as part of the CUD BPMALL display.

The CUD BPMALL display presents in succession what is being shown by each CUD BPM display that is set to CYCLE. Thus, DIFFTMT/ABSOLUTE and CYCLE/NOCYCLE have no meaning for the CUD BPMALL display as it is just a set of CUD BPM displays. (In fact, setting the CUD BPMALL display to CYCLE confuses the CUD software). Hence, to prevent confusion, the CUD BPMALL display has been changed so that CYCLE/NOCYCLE and DIFFTMT/ABSOLUTE is neither shown nor toggleable from the CUD BPM Panel.

- There has been a problem with the CUD BPM and BPMALL Displays that made it unwise to set their update interval to less than 120 seconds or so. This problem has been corrected; it is now possible to choose any update interval for the CUD BPM and BPMALL displays.

Damping Ring Watchdog Update

June 29, 1993

Author: *Ron Chestnut* **Subsystem:** *Damping Ring* **User Impact:** *Small*
Panel Changes: *None* **Documents:** *No* **Help File:** *None*

The two new slow feedback watchdogs monitoring the state of the RF in each damping ring have been augmented. These loops can be selected from the slow feedback panel. Similar to the polarization watchdog in PL01, these loops update status (FFBK,DR02,42,PSTA and FFBK,DR12,43,PSTA) which are used by the summary display as input to the PHAS/AMPL/etc. box for the damping rings. This status supercedes the previous AMPL checking in the damping rings.

If the RF system is in OFF or TUNE mode, the status is informational only and no SIP messages are sent. All error messages are marked as being from the North or South damping ring.

The status possibilities, from most to least severe, are as follows:

- Damping Ring RF forward power low
- Damping Ring RF forward power high
- Damping Ring RF gap voltage out of tolerance
- Damping Ring RF reverse power high
- Damping Ring RF gap voltage unbalanced
- Damping Ring Tuning Angle out of tolerance

The last item is reported only if the situation has been the case for four consecutive reporting times (about two minutes).

Phase Ramp + PSK Multiknob

June 29, 1993

Author: *Ron Chestnut* **Subsystem:** *EAST TUNE* **User Impact:** *Small*
Panel Changes: *Few* **Documents:** *No* **Help File:** *None*

A new multiknob has been created which moves the electron phase AND the PSK timing at the same time. The motivation was to remove the need to one-shot the energy-difference slow feedback loop when changing the phase. The [E- PHSRMP +PSK2] multiknob is available off the EASTTUNE panel, adjacent to the [E- PHSRMP MULTI] and [E+ PHSRMP PHAS 6] buttons. Since the PSK tracks slowly, and since the calibration of PSK vs. Phase is valid only over a small range, this knob is meant for small corrections only. Should it prove popular, a similar knob for [E+ PHSRMP +PSK2] can also be contrived.

Summary Display Lists

July 22, 1993

Author: *Ralph Johnson* **Subsystem:** *All* **User Impact:** *Small*
Panel Changes: *Few* **Documents:** *No* **Help File:** *No*

The SDS facility which is used to show the status of lists of devices included in summary boxes has been upgraded to support a last page button. It has also been changed such that the line numbers used to identify items are relative to the complete list of devices selected to be shown rather than relative to the display page. That is, as you go to the next page the numbers will increase rather than beginning at 1 for each page.