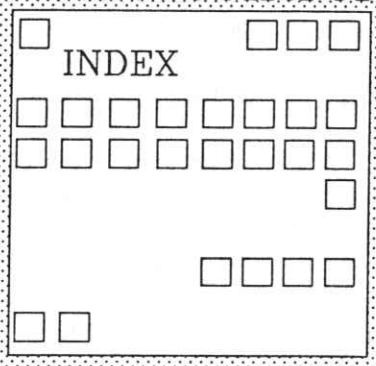
Index Panel

SLC Control Program



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SPECIAL MAGNET UPGRADE EDITION

Major Upgrade of Magnet Control Software

January 29, 1989

Author: *Nan Phinney* **Subsystem:** *All* **User Impact:** *Major*
Panel Changes: *Few* **Documents:** *Yes* **Help File:** *Old*

There has been a major upgrade of the magnet control software to implement recommendations of the Magnet Task Force and to fix a number of outstanding problems. Some of the changes are already in production and have been mentioned in previous Index Panel articles. The rest of the improvements will be released this week, except where specified as a future release. Because of the potential impact of these changes, we have dedicated a special edition of this newsletter to the new magnet software so that it may be referred to as a handbook.

1 Overview

A major problem during SLC commissioning has been the inability to reliably restore magnets to a previous configuration. The magnet task force has identified a large number of factors contributing to the lack of reproduciility, including inadequate hardware and software, incorrect database values, and poor operational procedures. The SLC software engineering group has worked closely with the magnet task force to define improved algorithms for setting magnets to reproducible fields and for providing robust diagnostics to identify problem supplies.

The most important feature of the new control algorithms is a much improved Trim procedure which 'Creeps up' to a setpoint to avoid overshooting. When possible, standardization is respected and the STDZ_OK bit is lost whenever the current is changed in the wrong direction. Individual Settling times are specified in the database for each device, allowing the software to wait long enough for a supply to stabilize after any change. The calibration procedure has additional checks on linearity and range and a new calibration diagnostic procedure will provide easier trouble-shooting for individual supplies. There are also a variety of improvements in performance and error handling, plus some new features, all described below.

2 New database values - SETL, HDSC, RAMP

SETL - Each power supply now has an individually specified Settle time to indicate how long the software must wait after a change before the readback is reliable. The database attribute, SETL, gives the settling time in milliseconds for a full scale change. For changes less than 10% of full-scale, a shorter wait time is used. All of the standard closed loop algorithms (Calibrate, Standardize and Trim) use the new SETL times. For initial commissioning, the database contains rather conservative 'long' settle times. These will

be tuned with further experience. The net effect of introducing SETL times is that some functions may take longer but the actions will be more reproducible. Some of the delays may be shortened when the optimal SETL times have been measured.

HDSC - A new Hardware DeSCriptor bit mask has been added to the database to provide extra bits for describing hardware ideosyncracies. It is displayed on the standard magnet display along with the HSTA and STAT masks. It contains static bits which may not be changed except by editing the database. Included are bits to describe new hardware such as the PSCII and PSCIII and old hardware such as ARC movers or triggered devices such as PAU channels or Kickers. They may also be used to support new features such as Remote Reset for some PSCs. Where possible without major software impact, some of the static bits previously included in the Hardware STAtus, HSTA, will also be moved to HDSC. Candidates are the PSC Reversible and Polarity bits, the bit to identify Shunted/Booster Quads, and the bit to specify Up vs Down polynomials. These changes will be made in a future release. (See Appendix below)

RAMP - The Ramp secondary previously used only for PSC-controlled devices has been extended to other supplies. For PSCs (LGPS in database) the Ramp values specify Slow and Fast ramp rates to be used with the PSC internal ramping feature. For all other devices, the two RAMP values will specify a maximum step size to be taken when changing the DAC and a wait time before the next step may be taken. These values may be used to protect supplies from going out of regulation in response to a large change in the control voltage. In particular, it may be used to protect the Blowtorch Quads which are now protected only by a software kluge. This feature will not be implemented in this release but the database slots have been added for future use.

3 TRIM algorithm

The magnet Trim procedure is at the heart of this major upgrade. Using the new Settle times, the software should always wait for the power supply to stabilize before reading back the current. For standardized supplies, the algorithm 'Creeps' to the new set point, typically in two or three steps. Once the device is within trim tolerance, a final pass is made to attempt to bring the device to its exact set point rather than leaving it near the limit of the trim tolerance. The most visible effect of this procedure is that most devices will have ITRY greater than one after trimming. Unless the requested setpoint change is contrary to the standardization direction, the STDZ_OK bit should be preserved and the device trimmed in at most three steps. Because of the care taken with settling times and the multiple steps, some Trim requests will take longer than before but should give more reproducible results. If a device appears to drift out of tolerance immediately after Trimming, the SETL time may need to be increased.

Another new feature incorporated in this release is that the slope of the DAC to Current transfer function is always used to calculate the new DAC setting. Previously the Trim software calculated the first DAC setting using both the slope and offset terms of DVI or DVIC. In the past this has caused some poorly characterized supplies to overshoot wildly on the first step of the trim. The new procedure will trim such supplies more smoothly but may generate more frequent DAC out of Range messages when trying to Trim a supply which is Off.

The magnet task force discovered a hardware problem with the POWER10 booster supplies used for QUADs in sectors 11 through 29. Most of the failures in these supplies have occurred when operating at greater than 10 amps (about half of the maximum current available). The algorithm for setting these supplies has been modifed to minimize the required operating current. (ref IP 2-74)

Lastly, a check has been added to determine that a supply is following the changes in DAC setting before proceeding to another step. A similar check has been used successfully with the ARC magnet movers. If the software detects that the change in the readback is less than 10% of the requested change, an error message will be issued and the DAC will be restored to its previous setting. With the old software, if the device did not respond, the Trim would continue to iterate up to ten times, increasing the DAC setting with each

pass and increasing the likelihood of hardware failures when the device was eventually turned on. The new algorithm is particularly important for protecting Kickers and other triggered devices. It also means that an attempt to trim untriggered or offline devices will abort after only two steps, one trim and one reset.

4 STANDARDIZE algorithm

The magnet task force has noted that many supplies drift as their temperature stabilizes after they are set to operating current. Such devices may be set more reliably if they are trimmed immediately after standardization when they are already at operating temperature. To this end, the normal Standardize function now performs a Standardize followed by a Trim (ref. Kirby, Index Panel 2-74). After a standardization request, the supplies should be left at the desired setpoint with the STDZ_OK bit set. If required, a Standardize Only function is available on the diagnostic panel.

Greater care has been taken throughout to ensure that the STDZ_OK bit (60 Hex in STAT) is meaningful. The bit is set at standardization and cleared whenever the DAC is changed opposite to the hystersis direction by any of the standard procedures such as Trim, Calibrate, Perturb, or Dac Zero. It is also cleared for a variety of Camac problems or whenever a Check finds that the device is more than a check tolerance away from its previous Trim current in the wrong direction. This last logic picks up devices which have tripped off or been moved with a Diagnostic knob. Previously, STDZ_OK was lost only when devices were knobbed or turned off. Users should be aware that the absence of the STDZ_OK bit does not mean that the device did not Standardize successfully but only that standardization has not been maintained. (ref IP 2-74) The last successful Standardize time is available in the KTIM secondary on the single unit display or from the Designer Zplot panel.

Correct handling of the STDZ_OK bit has necessitated some changes in the operation of certain supplies. The STDZ_OK bit is now set at standardization for the individual Linac shunt and booster Quads as well as for their bulk supply. If a bulk Quad supply loses standardization, so do all of the associated Quads. If the shunted supplies are to maintain standardization, their bulk supplies must be set going down from maximum current with the shunts supplies subtracting additional current afterwards. Another problem was found with bipolar supplies such as the ARC and Final Focus correctors which were previously left at zero after standardization. On the average half of the supplies moved against the defined hysteresis direction on the first trim and lost STDZ_OK. To avoid this the standardize cycle has been changed to leave the supplies at the lower limit after standardization. Similar problems will need to be corrected elsewhere as they are discovered.

There are two more minor changes to Standardize. The procedure now ensures that supplies are left at their specified final current even if they fail some step of the standardization. Previously, that supply would simply be dropped from the control list, possibly leaving a supply at high current. The algorithm now also recalculates the needed wait time at each step of the cycle, guaranteeing that the procedure no longer waits for slow supplies which may no longer be standardizing. (ref IP 2-74) The wait time needed for any supply is always the larger of the specified SETL and NSCY times.

5 CALIBRATE algorithm

The Calibrate procedure measures the DAC to Current transfer function, DVIC, and verifies that a supply is performing as designed. It should be a powerful tool for detecting and diagnosing problem supplies. In the past the Calibrate function has been used for initial commissioning of a system, but rarely afterwards. The magnet task force has found supplies that have not been calibrated since 1986. Also many devices have calibrate tolerances, ATOL, set so loosely that even malfunctioning supplies calibrate successfully. If the system is to produce reliable magnet settings, calibration tolerances and checks must be tightened up and the procedure must be run frequently so that supplies are well characterized and so that problems are quickly detected.

A new Calibrate Diagnostic procedure is being developed to assist in tuning database parameters for each supply and to help in diagnosing hardware problems. This is described in a separate section of this newsletter.

Normal Calibration has been modified to use 6 steps instead of 5 in order to avoid a step at zero for bipolar supplies which may not regulate well at low voltage. This will slightly increase the time taken by the Calibrate cycle, as will the use of the individual settle times. It should produce a more reliable measurement of the DAC to current transfer function, DVIC, which must be well understood for the new Trim procedure to avoid overshooting. To recuperate some of this increase in time, a fast/slow ramp cycle has been added for the first step of a PSC calibration and also when setting the PSC before and after calibrating Shunt or Booster Quads.

As noted above, some of the standardize and calibrate cycles specified in IMMS have been modified in order to allow supplies to maintain standardization while trimming. In some cases the final setpoint after standardization, IMMS(3), has been set to full current so that any trim is in the preferred direction. In the previous version of the magnet software, this value has also been used to specify the final setpoint of a calibration cycle. In this release, the DAC is set to zero at the end of calibration for all devices except Stepping motors and Movers which still use IMMS(3) as a final setpoint. This should reduce the risk of hardware failure when supplies are left at full current for an extended period.

New checks have also been added to help identify hardware problems. The DVI Goodness value in the database, DVIG, now contains the average residual error from the linear fit to the 6 steps. For properly functioning hardware with correctly chosen database limits and settling times, this number should be small. It essentially measures the non-linearity of the measured points. For this release, it is merely calculated and stored in the database. Checks and error signalling will be added after there is some operational experience to determine reasonable tolerances to use.

At the end of calibration, the software calculates the DAC settings needed to reach the full current range specified in IMMS and IMMO using the new DVIC. If any limit results in a DAC setting exceeding the number of bits available, a warning message is issued.

In a future release, the time stamp for last Calibration will also be checked before any device is Standardized and the user will be prompted to reCalibrate if the Calibration is too old.

6 New Error Handling

New logic has been introduced to warn the user if all of the devices selected for a particular Calibrate, Standardize, etc. function have that function disabled. A new message is issued stating that no action has been taken. (ref Kirby, IP 2-74)

A long standing problem has been that error messages were often generated by CAMAC or database problems on a device other than the one or ones of interest. This made it difficult for higher level applications to know whether a bad return status on a Check or Trim function was relevant. In this release, CAMAC error handling has been changed so that errors are only reported if they affect one of the devices selected for Trim, Calibrate, etc. (ref IP 2-74) Similar changes have been made in the reporting of database problems or bad polynomials.

Pulsed devices controlled by a PAU have a status bit which indicates that the readback has not been latched since the last time the DAC was set. This has been indicated on the standard magnet display by a red status and the error string ADCERR. It will now be reported as a warning (Yellow) condition with the string NoTrigger. (Cater 5158)

The standard magnet values display has been updated to include a column for the HDSC secondary. In order to make room, the error text field and the RMS text have been combined and RMS is only reported if no other error is present.

The magnet adjust and diagnostic knob routines now check that a device is Online before assigning a knob. This test had been overlooked in the previous version and has caused some operations confusion. (CATER 5602) There was also a bug found in the knob routine's handling of Shunted or Booster Quads which has been fixed. The gain factor for these knobs has also been reduced to match their limited range. Another old problem is that knobs would seem to get lost if once requested to go out of DAC range. The error recovery for this fault has been improved so that knobs should continue to follow smoothly once the requested value is back in range.

7 Enhanced PSC Control

The new software will support the PSCII, with a 16 bit DAC and ADC and slower ramp rates. It is implemented in this version of the micro software but not tested, so further improvements may be necessary before it is fully operational. The slowest ramp rate available on the PSCII is over 1000 seconds for a full-scale change, making operations such as calibrate or standardize rather arduous.

A new Remote Reset function will be supported for designated PSCs. The procedure will only be enabled for supplies with the appropriate bit set in the new Hardware Descriptor mask, HDSC. The supply will first be turned off and then a reset issued using the second pulsed output bit from the PSC.

There will be a hardware modification to the interface chassis for PSCs controlling pulsed devices so that a status bit will be available to indicate whether the device is receiving triggers. Such devices will be indicated by a bit in HDSC. The trigger On/Off information will be wired into the PSC Polarity input bit used by reversible supplies. This status may be used to prevent attempts to change the DAC while the supply is not being triggered.

The DAC Zero procedure for PSCs has been modified to use the database specified fast ramp rate to run the supply to zero. This may reduce the time required to set Access.

Similar logic to make a two step ramp has been added to the Degauss procedure used to Degauss 50B1 when switching from SLC to PEP/SPEAR mode. In the future, the Degauss function will also be available from the Access Control procedures to speed up and simplify switchover.

The first generation PSC module has a second analog input to measure Ripple. This is now routinely read out every 10th check function, converted to equivalent current, and updated in the RIPL database entry. Similar code converts the Ripple bits from a SAM module into current and updates RIPL for SAM/DAC devices. In the future, these values may be checked and an error reported for devices with excessive RIPL. This awaits operational experience to define reasonable tolerances.

8 APPENDIX

Proposed arrangement of Hardware DeSCriptor (**HDSC**) and Hardware STAtus (**HSTA**) bits. Where marked with an arrow <, the currently defined HSTA bit wlll be shifted into the HDSC word in a future release.

BIT	HDSC(Descriptor)		HSTA(Hdwe Status)	STAT(Status)	BIT
0001			In Service	GOOD Status	0001
0002				WARNING	0002
0004			OFFLINE	OFFLINE	0004
0008				IN TROUBLE	0008
0010			Turned OFF	OFF	0010
0020	Polarity Reversed	<	Polarity Reversed	Standardize OK	0020
0040	Reversible Supply	<	Reversible Supply	Calibration OK	0040
0080	PSC RESET OK		BAD RMS		0080
0100	PSC 2		Calibrate Disabled	Database Error	0100
0200	PSC 3		Perturb Disabled	DAC Error	0200
0400			Trim Disabled	ADC Error	0400
0800	PAU or Pulsed PSC		Standardize Disab.	Out of Range	0800
1000	ARC Mover		No Retry on Trim	Out of Tolerance	1000
2000	Magnet uses IVBD	<	Magnet uses IVBD	Bad Ripple	2000
4000	Shunt/Booster	<	Shunt/Booster	Bad BACT	4000
8000			No AUTO Trim		8000

Magnet Calibration Diagnostics

January 29, 1989

Author: *Ken Underwood* **Subsystem:** *Magnets* **User Impact:** *Some*
Panel Changes: *None* **Documents:** *Yes* **Help File:** *Yes*

Reliable operation of the SLC demands that the magnetic fields throughout the system are stable and reproducible to very tight tolerances. The Magnet Task Force has developed a hardware test setup to analyze the dynamic behaviour of individual supplies and identify problems. This setup is very powerful but too clumsy and time-consuming to be used on every supply.

A new Calibration Diagnostic procedure has been developed to allow detailed study of the dynamic response of an individual supply directly from the SCP. This is not yet available but will go into production in the near future. The diagnostic calibrate mode can be used with only one power supply at a time and is accessed from a special Calibrate Diagnostic Panel selected from the Magnet Diagnostic Panel. During the Diagnostic Calibrate, new software in the micros collects additional ADC, DAC and time values during the Calibrate cycle and returns them to the VAX for display. The VAX interface software provides two different diagnostic calibrate modes, **REFERENCE** and **SAMPLE**, with appropriate graphical displays.

The **REFERENCE** diagnostic calibrate mode is a conventional calibration but the DAC, ADC and time values for each point are returned to the VAX. The number of steps can be set by the user (4 to 20; default 10) Two displays will be available in this mode. The first will plot the power supply current vs. DAC value. The second will plot the error in power supply current vs. the DAC value and the difference between the DVI and DVIC polynomials vs. the DAC value.

The **SAMPLE** diagnostic calibration mode also performs a conventional calibration but in addition, collects a series of sample points immediately following the setting of the DAC for SAM/DAC power supplies and following the ramp for PSC power supplies. The number of points (4 to 20; default 10), the number of samples per point (5 to 20; default 10) and the wait time (250 to 1000 msec; default 250) can be specified by the user. Only one type of display will be available in this mode and will plot a detailed view of the current vs. time for each of the sets of samples.

The diagnostic calibrate will also calculate and update the new (DVIC) current to DAC polynomial and the (DVIG) residual DAC error in the database. These new values will be displayed on each of the plots.